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Introduction To SemiConductor theory.

Solids can be classified upon their electrical conductivity.

Insulators:- Insulators are the substances that do not allow flow of carriers through them.

Ex: wood, glass, diamond.

Atoms have tightly bound electrons that are static and do not move.

Conductors:- are materials that allow current to flow through it. Charge carriers electrons move easily from atom to atom. It offers little or no resistance to flow of current.

Ex: metals, table salt.

SemiConductors:- Materials having properties between conductors and an insulator.

ex: Germanium, Silicon.

SemiConductors:-

→ Resistivity of semiconductor is less than insulator but more than conductor.

→ With increase in temperature

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resistivity decreases, hence conductivity increases.

→ Suitable impurity like Gallium, Arsenic can be added to semiconductor to change towards conductor.

Types of SemiConductor

→ Intrinsic SemiConductor :- SemiConductor in a pure form. Ex: Germanium (Ge), Silicon (Si).

→ Extrinsic SemiConductor :- Impurities are added to ~~the~~ pure SemiConductor, i.e, Si ~~added to~~ is called Extrinsic SemiConductor.

The process of adding impurities is called Doping.

Impurity can be trivalent (3-valence e⁻) or pentavalent (5-valence e⁻).

→ Types of Extrinsic SemiConductor :-

→ N-Type :- When a small amount of pentavalent impurity (ex: Ph, Arsenic) is added to pure semiconductor then it is called N-type.

Here electrons are majority carriers

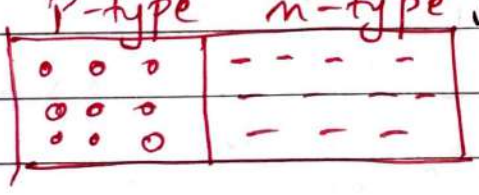
and holes are minority carriers.

→ P-type :- When a small amount of trivalent impurity (Boron, Al) is added to pure semiconductor then it is p-type semiconductor.
Here holes are majority charge carriers and electrons are minority carriers.

Note: In N-type semiconductor current is due to flow of electrons
In p-type semiconductor current is due to flow of holes.

P-n junction:

A P-type semiconductor & n-type semiconductor brought together, and system is heated to temp of 500°C & then temp is lowered to form a single slab. This is called p-n junction



p-type has holes as majority carriers. n-type has electrons as majority carriers.
Due to concentration gradient

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In both the material, holes move towards n-side & electrons from n-side move towards p-side. This process is called Diffusion.

The junction formed between p- and n type is called pn junction.

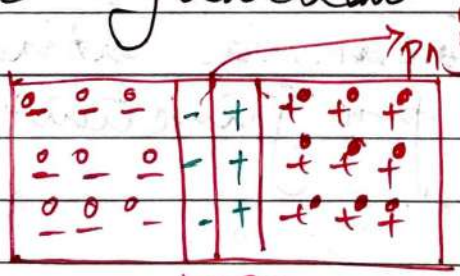
The electrons from n type move to p-type recombine with holes and become -ve charged immobile ion.

The holes from p-type move to n recombine with electrons and become +ve charged immobile ion.

Thus immobile ions are formed across the junction.

These immobile ions form a layer across the junction called the Depletion layer.

This layer prevents further movement of charges across the junction.



Operation of pn junction is under 3 diff cases

→ No Bias

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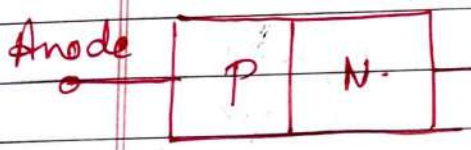
→ Forward Bias
→ Reverse Bias.

→ **No Bias:** under no bias condition potential barrier is created across the junction. This potential prevents further movement of charge carriers across the junction.

→ ~~Forward Bias~~:

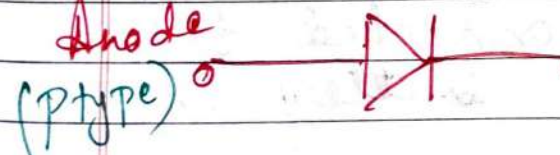
Pn junction Diode:

The term diode refers to two-terminal device.



Symbolic representation of diode. It has two terminals Anode and cathode. Anode refers to +ve terminal & cathode refers to -ve terminal.

Symbol of Pn Diode:



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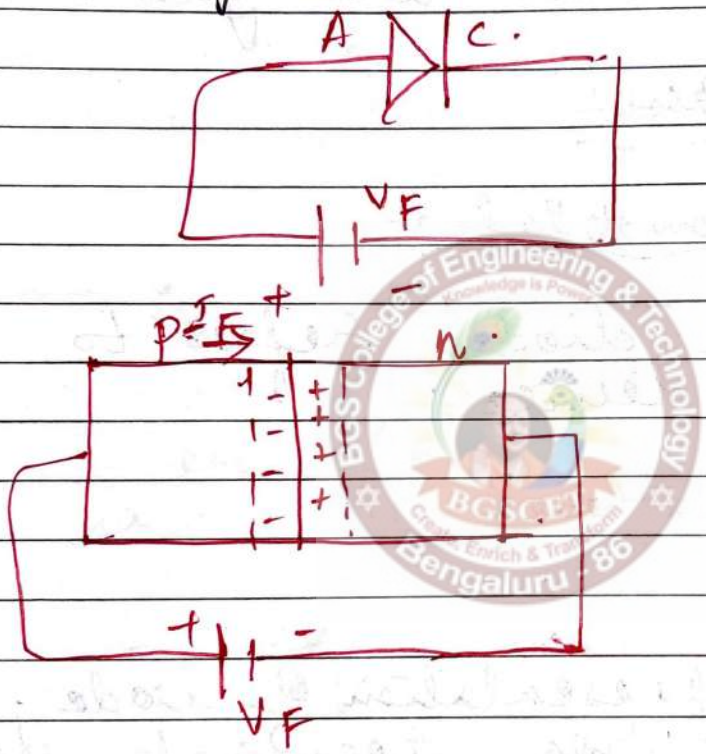
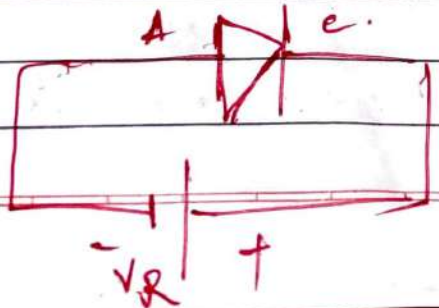
→ Forward Bias :-

Diode is said to be forward bias when positive terminal of battery is connected to p-type and negative terminal of battery is connected to n-type.



→ Reverse Bias :-

Diode is said to be reverse bias when anode is connected to -ve terminal of battery & cathode is connected to +ve terminal of battery



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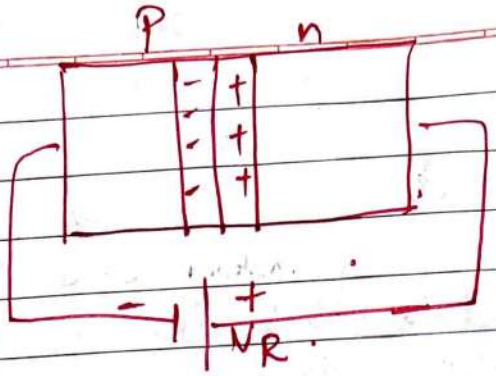
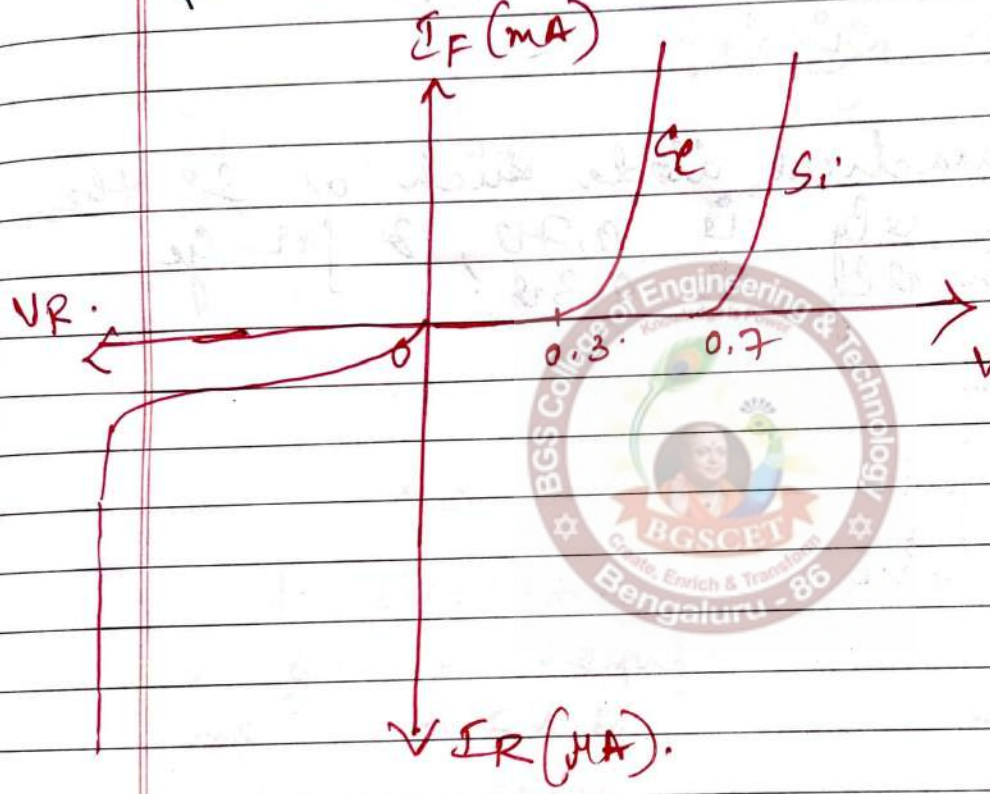


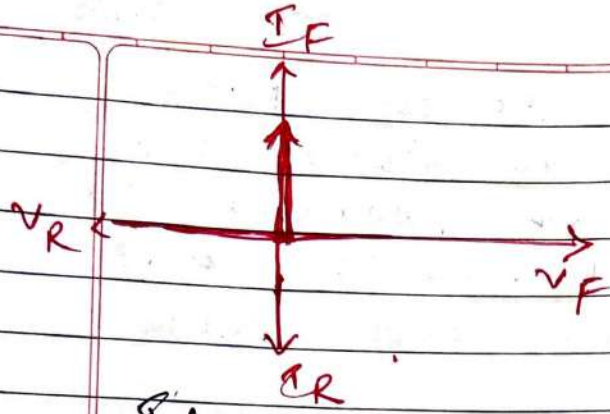
V-I Characteristics of Diode :-



→ **Diode Approximations :-**

Diode has low resistance under forward bias and high resistance under reverse bias.

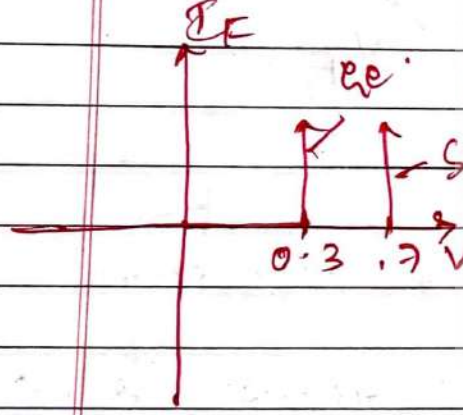
Ideal Diode :- This has zero forward resistance and zero cut in vtg.



Ideal diode.

→ Practical diode:-

In practical diode such as Si the cut in volt is 0.7V, & for Ge cut in volt is 0.3V.



→ Zener diodes:-

When a diode is reverse biased, very small current flows due to minority carriers. If reverse bias is increased junction breaks down and current increases. This results in breakdown of pn junction diode.

A pn junction silicon diode which is heavily doped & designed

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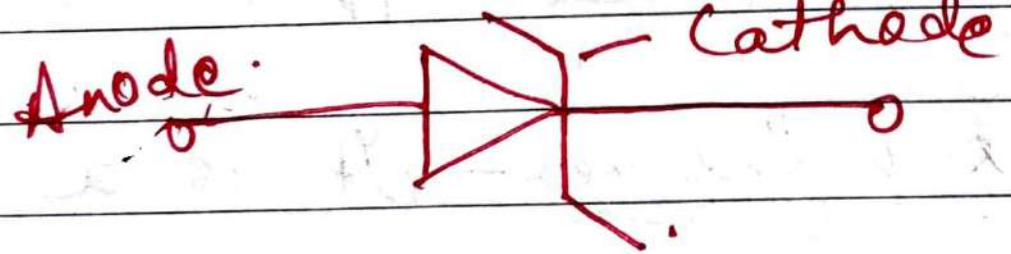
to operate under reverse bias condition is called Zener diode.

Such diodes are stable over wide range of current & but maintain constant voltage across the device.

In Zener diode reverse current is limited by external resistor.

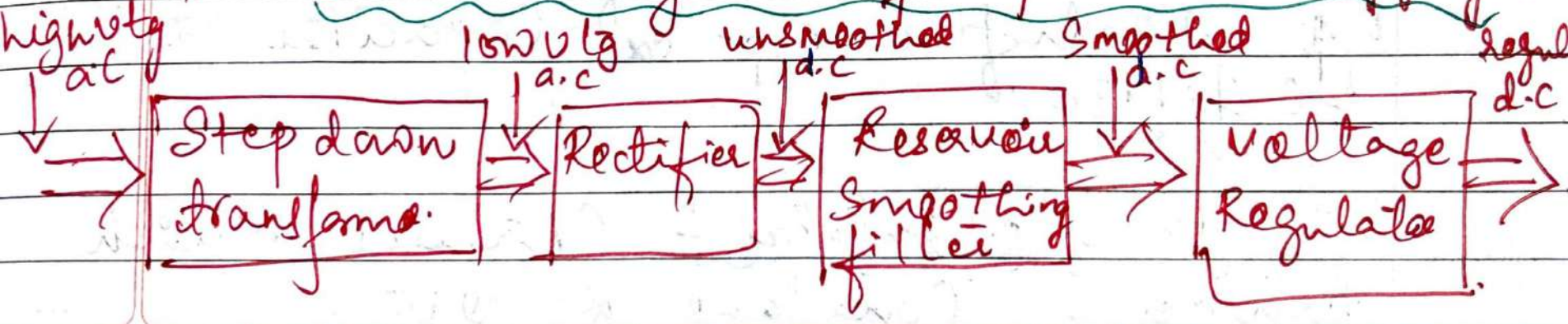
Symbol of Zener Diode :-



Module 1: Power Supplies:

All electronic circuits require a source ..regulated dc at voltages between 5V & 30V. In some cases this supply can be derived directly from batteries (ex: 6V, 9V, 12
In many cases it is desirable to make use of standard a.c. mains.

→ Block Diagram of power Supply :-



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Block diagram of dc power supply is as shown.

Input mains is at relatively high vtg a step down transformer of appropriate turns ratio is used to convert it to low vtg.

This low vtg is then rectified using diodes to produced dc output.

This dc o/p is then filtered to get smoothed o/p.

→ Step Down Transformer :- It is a device that has two coils windings : primary & secondary used to convert high vtg (230V / 50Hz) to low ac vtg.

→ Rectifier :- It is a device with one or more diodes. It converts secondary Ac vtg to pulsating Dc.

→ Smoothing filter :- It is a filter used to remove fluctuations (ripples) in rectifier o/p ex: Capacitor filter, LC filter.

→ Voltage Regulator :- Circuit which provides constant dc vtg.

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Rectifiers:-

Semiconductor diodes are used to convert ac to dc. Such devices are called Rectifiers.

There are diff types of rectifiers
Half Wave Rectifier (HWR)
Full wave Rectifier (FWR)
Bridge Rectifier.

→ Half Wave Rectifier:-

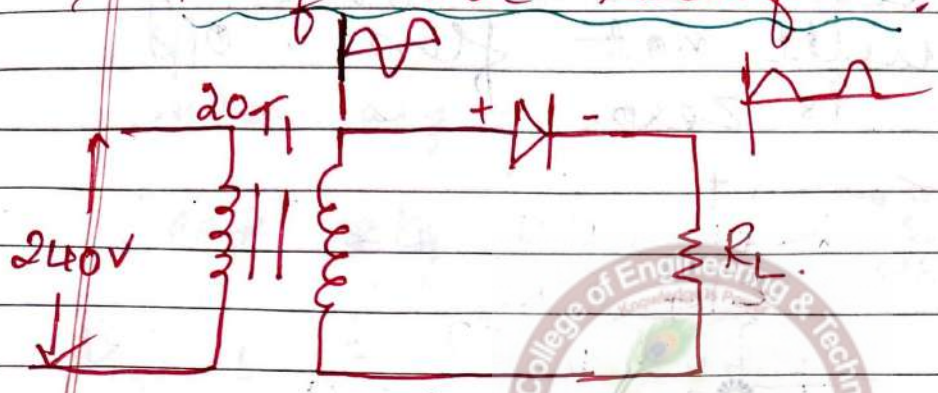


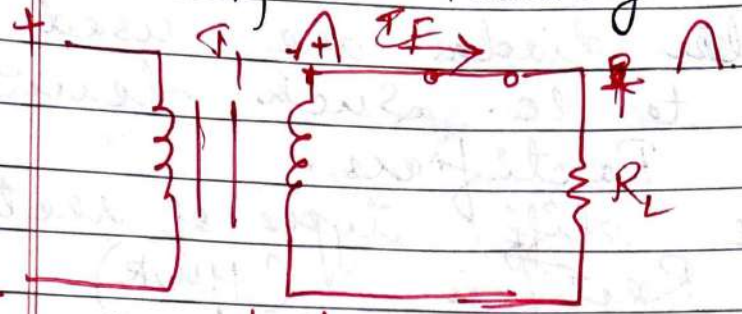
fig shown half wave rectifier. Mains vtg 240V is applied to the primary of a step down transformer (T_1). The secondary of T1 steps down 240V rms to 12V r.m.s. The turns ratio is 20:1.

So $\frac{240}{20}$ = 12 V r.m.s obtained at secondary of the transformer

During +ve half cycle of i/p:-

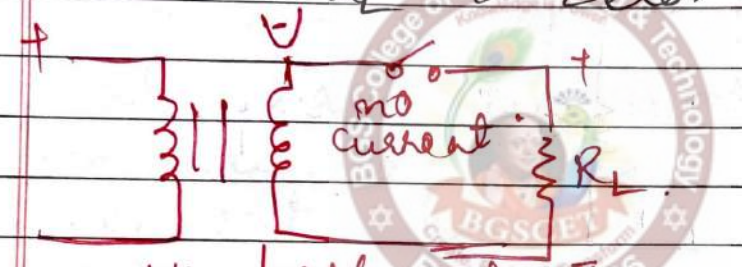
During +ve half cycle of i/p diode conducts. It acts as

closed switch. It allows current to flow through it. O/p is +ve half cycle.



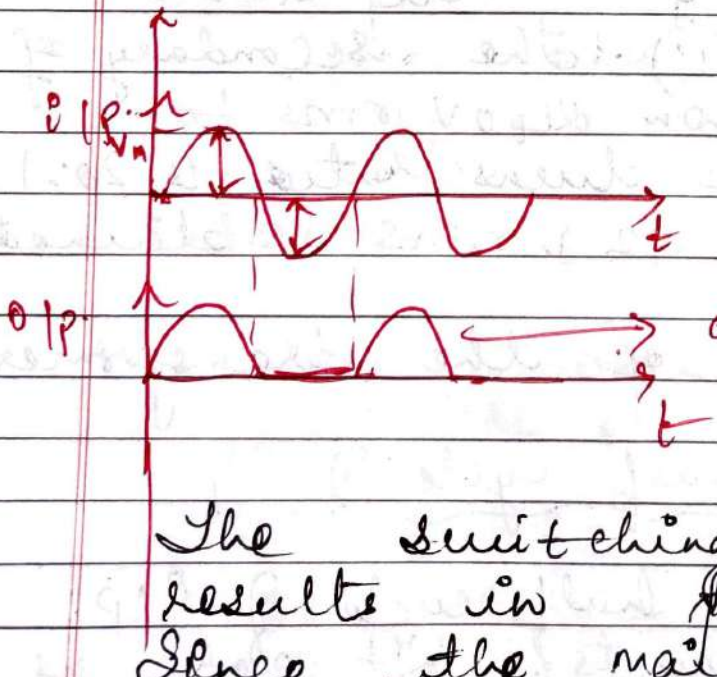
+ve half cycle

During -ve half cycle of i/p diode is reverse biased. It is open current will not flow. O/p across R_L is zero.



-ve half cycle

The o/p of HWR is



The switching action of diode results in pulsating dc o/p. Since the mains supply is 50Hz

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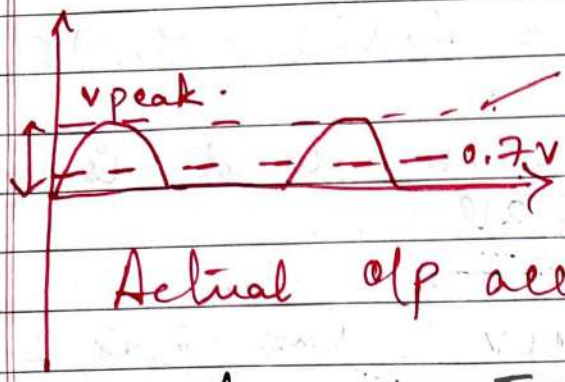
the o/p across R_L is also 50Hz. The Si diode will drop 0.6-0.7 during forward bias.

→ Analysis during +ve half cycle:-



Actual o/p across the load.

Secondary of T_1 12V rms.

peak vtg across secondary

$V_{peak} = V_{RMS} \times \sqrt{2}$

$= 12 \times \sqrt{2}$

$= 16.96 \simeq 17V.$

$V_{peak} = 17V.$

diode drop is 0.6 - 0.7V.

so $17 - 0.7 = 16.3V.$

Actual o/p across the load is 16.3V.

Example:- A mains transformer having turns ratio of 11:1 is connected to 220V rms. mains supply. If secondary o/p is applied to HW R

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determine peak vtg across the load.

Solution :-

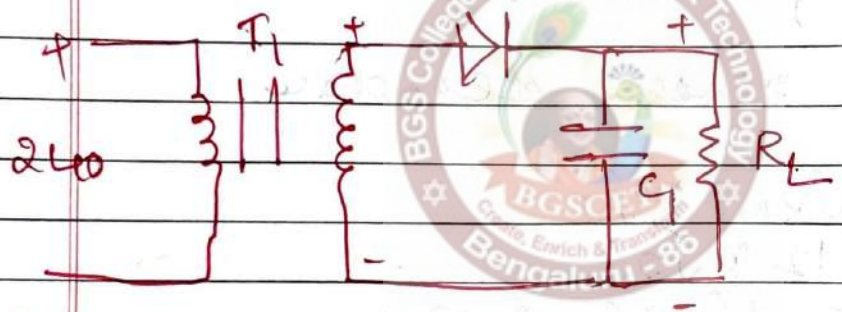
$V_s = \frac{220V}{11} = 20.$

peak vtg $V_{peak} = 20 \times \sqrt{2} = 7.07V.$

Voltage across the load is

$7.07 - 0.7 = 6.3V$.

→ HWR with Reservoir Capacitor :-



HWR circuit can be improved by adding a capacitor.

The o/p from the diode will charge the capacitor C_1. The c/f is connected in parallel to R_L. It is used to remove fluctuations (ripples or ac) present in rectifier o/p.

The capacitor C_1 charges to 16.3 V at the peak of the +ve half cycle. The voltage across R_L is same as C_1.

During +ve half cycle of secondary vtg diode is forward

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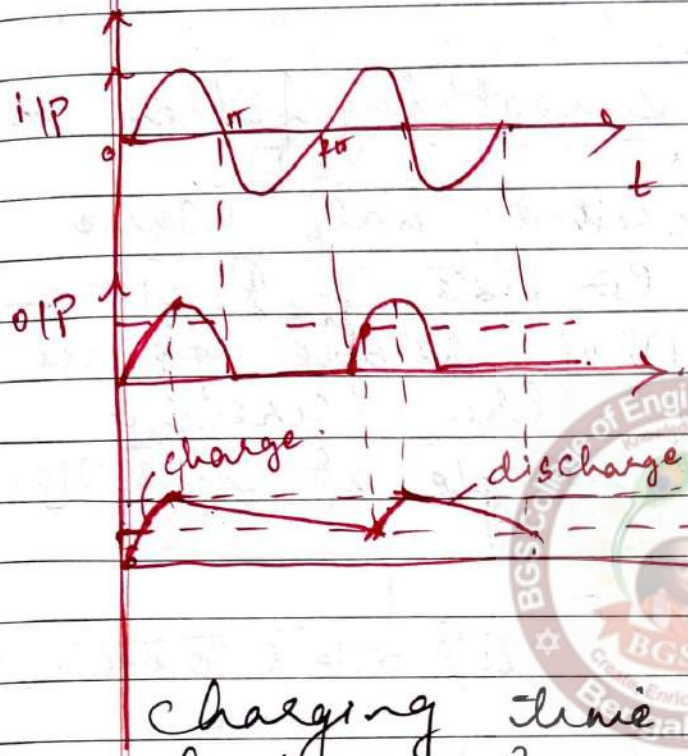
biased C_1 charges as rectifier o/p vtg increases to peak value (16.3 v).

When rectifier o/p starts to decrease C_1 discharges slowly through R_L until next +ve half cycle.

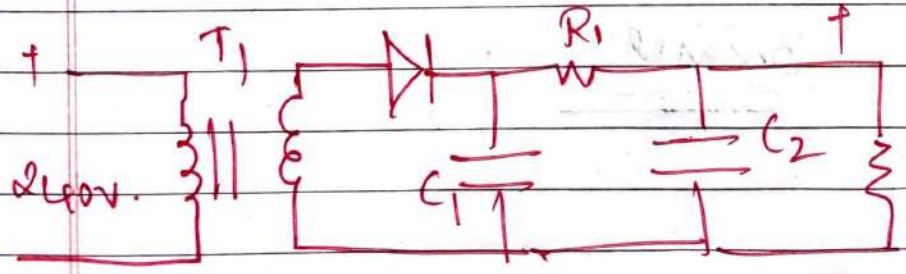


Discharging time of C_1 = $R_L \times C_1$.

Charging time of C_1 to the peak = $R_{series} \times C_1$

$R_{series} = R_{secondary} + R_{diode} + R_{wiring\ connection}$

Further refinement can be done by employing additional component C_2 & R_1. acts as filter to remove the ripples.



R-C Smoothing filter

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The amount of ripple reduced by a factor equal to

$$\frac{X_C}{\sqrt{R_1^2 + X_C^2}}$$

Example: The RC smoothing filter in a 50Hz main operated half wave rectifier circuit consists of $R_1 = 100\Omega$ $C_2 = 1000\mu F$. If 1V of ripple appears at the o/p of the circuit determine the of ripple at the o/p.

Sol: $X_C = \frac{1}{2\pi fc} = \frac{1}{2 \times 3.14 \times 50 \times 1000 \times 10^{-6}}$

$$X_C = 3.18.$$

$$V_{ripple} = 1V \times \frac{X_C}{\sqrt{R_1^2 + X_C^2}}$$

$$= 1 \times \frac{3.18}{\sqrt{(100)^2 + (3.18)^2}}$$

$$= 32mV.$$

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→ Capacitor as Reservoir:-

C_1 is referred as Reservoir capacitor. It stores charge during +ve half cycle and releases during -ve half cycle. Thus maintain constant o/p v.tg across R_L.

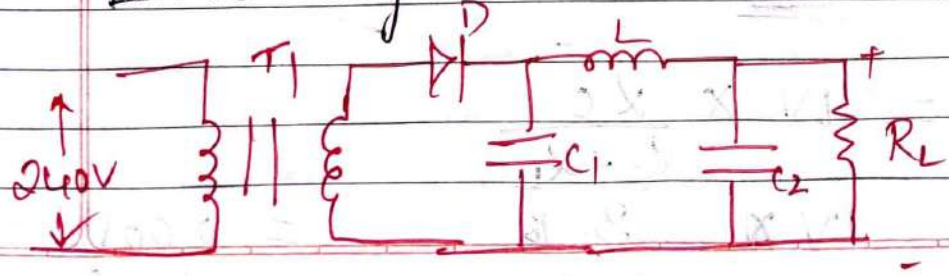
The ripples at the o/p can be reduced by choosing larger C_1 value.

→ Limitations of C-filter:-

If the capacitor value is increased to a high value the amount of current reqd to charge capacitor will be high. Diodes are subjected to high currents. So there is limit on increasing capacitor value.

→ Improved Ripple Filters:-

A further improvement can be achieved by using an Inductor (L1) instead of resistor (R_1) in the smoothing circuit.



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L_1 exhibits high value of inductive reactance while C_1 exhibits low value of capacitive reactance.

So L_1 bypasses remaining ac components

C_1 bypasses most of ac components. L_1 allows most of dc components.

This combined effect reduces amplitude of the ripple.

Example: The LC smoothing filter in a 50Hz mains operated HWR circuit consists of $L_1 = 10H$, $C_1 = 1000\mu F$. If 1V of ripple appears at the i/p of circuit, determine the amount of ripple appearing at the o/p.

Sol:

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2 \times 3.14 \times 50 \times 1000 \times 10^{-6}}$$

$$X_C = 3.18.$$

$$X_L = 2\pi fL$$
$$= 2 \times 3.14 \times 50 \times 10$$
$$= 3140.$$

$$V_{ripple} = 1V \times \frac{X_C}{X_C + X_L}$$

$$= 1V \times \frac{3.18}{3.18 + 3140} = 0.001V \text{ or } 1mV.$$

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Note: 1. Low capacitive reactance - When f approaches ∞, it acts as perfect conductor

2. When $f \to 0$ capacitor reactance will increase & acts like huge resistance.

→ Full Wave Rectifiers:

There are 2 types

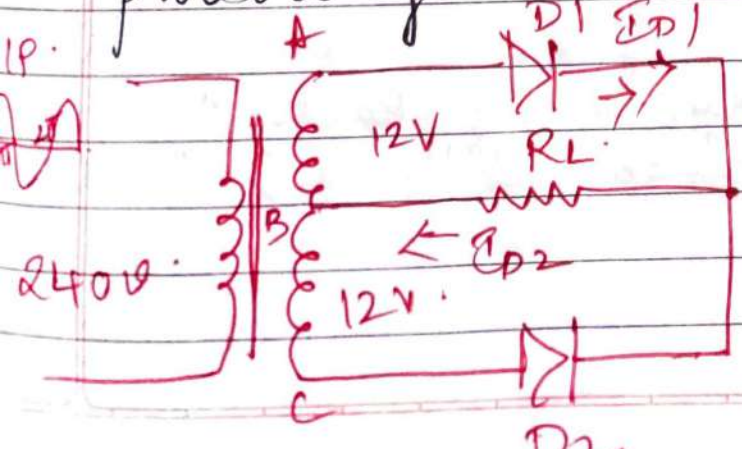
→ Biphase or Center Tapped full wave Rectifier

Uses two diodes and center tapped transformer.

→ Bridge full wave Rectifier: Uses four diodes & ordinary Transformer

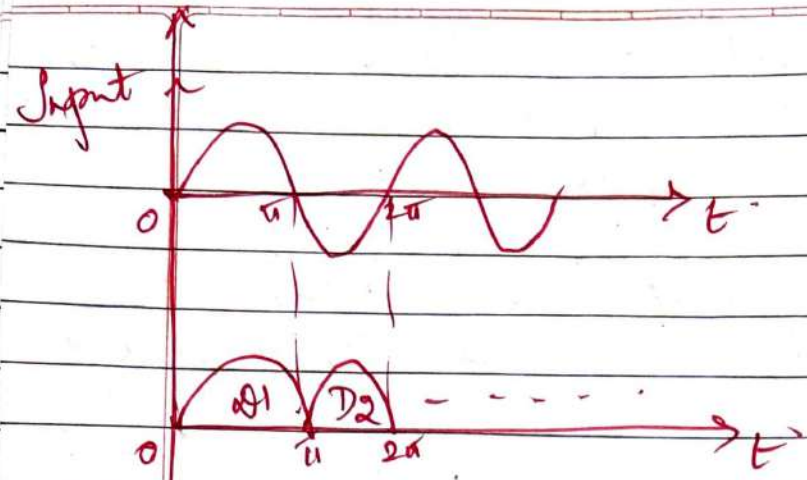
→ Bi-phase Rectifier:

The a.c mains 240V is applied to primary of T1 which has two identical secondary windings each providing 12V rms.



$\frac{240}{20} = 12.$

for turns ratio of 20:1.



→ On +ve half cycle point A is +ve w.r.t point B. Similarly point B is -ve w.r.t point C. So D1 will be forward bias acts like closed switch. D2 is reverse bias and is open switch. D1 alone conducts for +ve half cycle.

→ On -ve half cycle point A is -ve w.r.t to point B. Similarly point B is +ve w.r.t point C. So D2 will be F.B. acts like closed switch. D1 is reverse bias. D2 alone conducts for -ve half cycle.

→ The W/F's are as shown above.

Note :- ① V_{peak} produced by each of secondary windings $17 - 0.7 = 16.3\bar{V}$.

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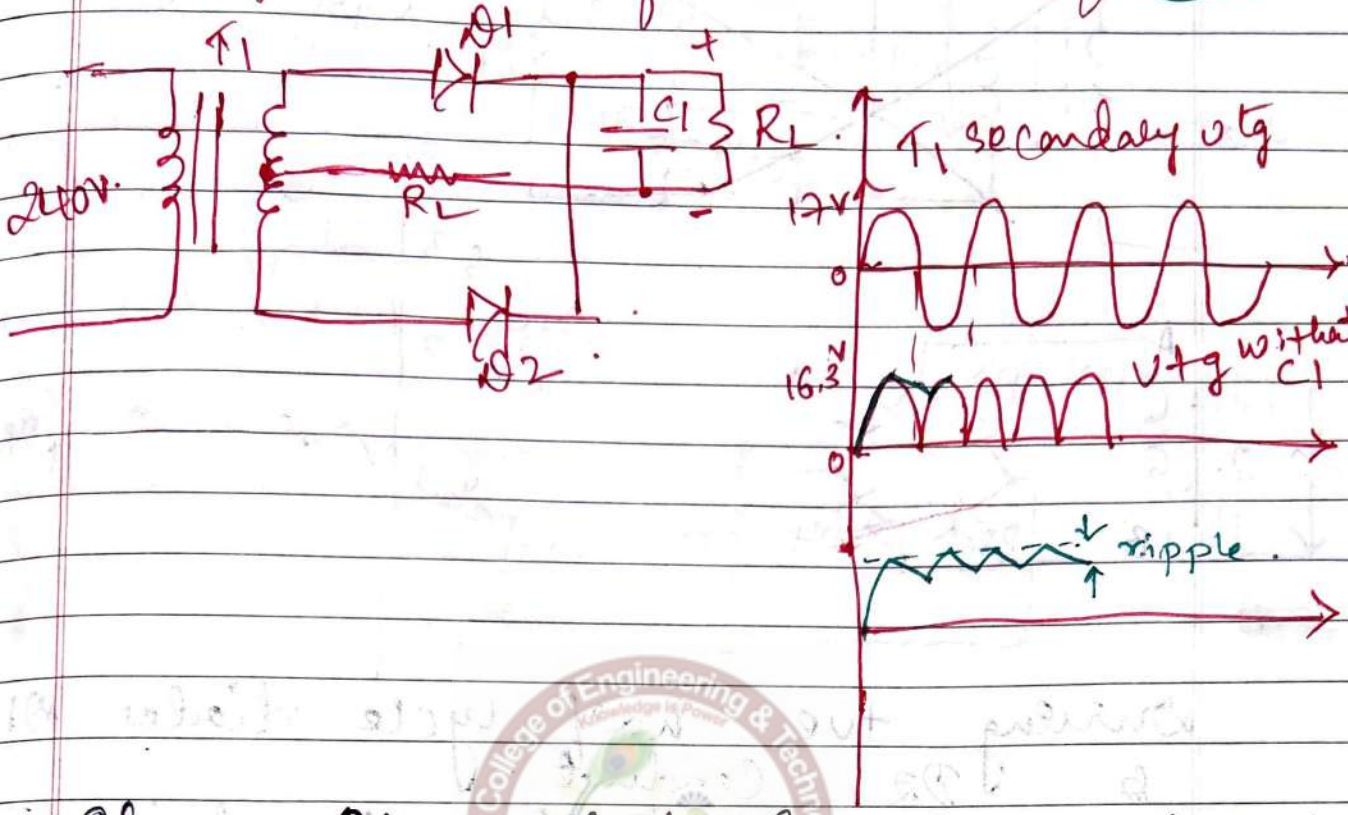
→ Bi phase Rectifier with C- filter :-

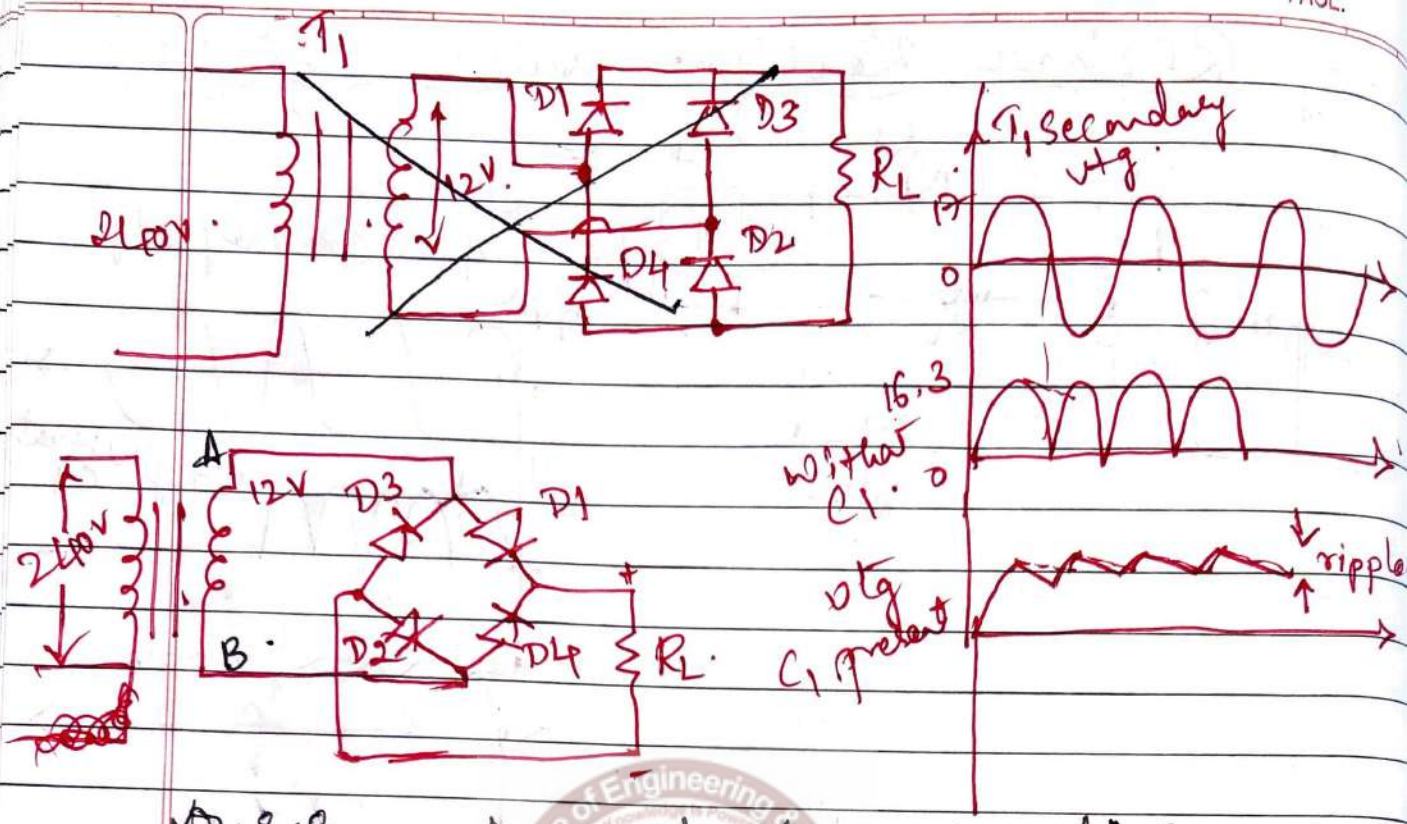


When D1 conducts C1 chaeges to peak 16.3V of the +ve half cycle. When D2 is in non-conducting state C1 dischaeges slowly through RL. when

When D2 conducts C1 chaeges to peak of -ve half cycle and C1 starts to discharge.

→ Bridge Rectifiers :-

Bridge rectifier ckt employs 4 diodes but only 2 diodes conduct during each half cycle. The ac. mains 240V is applied to primary of T1 & secondary windings provide of 12V rms.



During +ve half cycle diodes D1 & D2 conduct.
During -ve half cycle diodes D3 & D4 conduct.
The o/p across load with that C is as shown.
The o/p with C charging & discharging o/p is shown above.

→ Voltage Regulators:-

Voltage regulator is a device by which o/p vtg V_o is maintained constant regardless of change in i/p vtg or R_L. The circuit of Zener diode as voltage regulator is shown.

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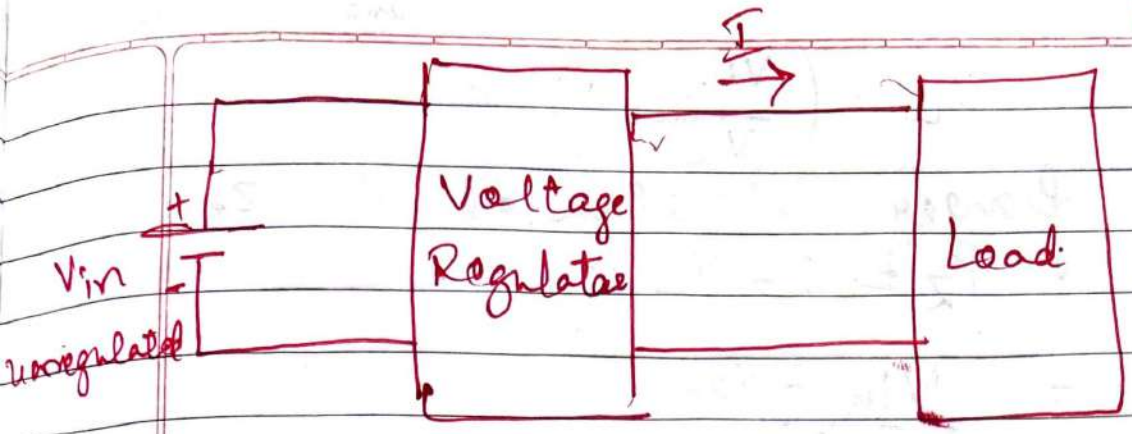

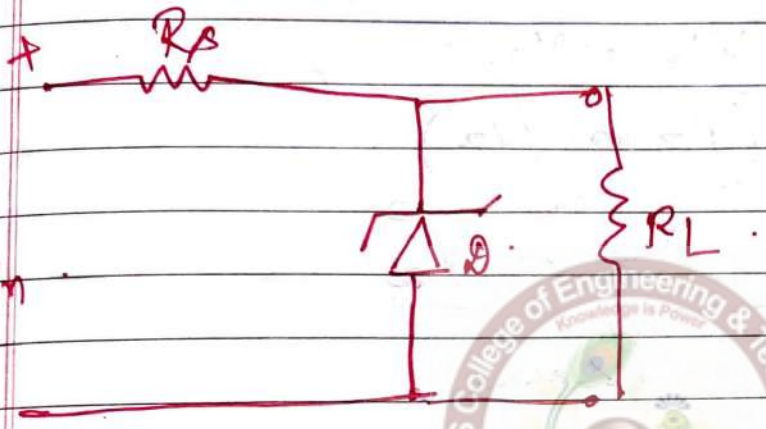

(I_Z = 2-5mA)

The series resister R_s is connected in the circuit to limit the current through zener diode to a safe value.

When RL is connected, zener current I_Z will reduce as current ($I = I_Z + I_L$) is split into load RL. O/p vtg V_o remains constant until regulation fails at current & produces lower than V_Z vtg

$$V_Z = V_{in} \frac{R_L}{R_L + R_S}$$

V_{in} is unregulated i/p vtg.

Max value of R_s

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$$R_{S max} = R_L \cdot \left(\frac{V_{in}}{V_Z} - 1\right)$$

The power dissipated in zener diode $P_Z = I_Z V_Z$.

$$R_{S min} = \frac{V_{in} - V_Z}{I_Z}$$

$$R_{S min} = \frac{V_{in} - V_Z}{(P_{Z max}/V_Z)}$$

$$R_{S min} = \frac{V_{in} V_Z - V_Z^2}{P_{Z max}}$$

→ A 5V zener diode has a max rated power dissipation of 500mW. If diode is to be used in simple regulator ckt to supply a regulated 5V to a load having a resistance of 400Ω. Determine suitable value of series resistor for operation in conjunction with a supply of 9V.

Sol^n: $R_{S max} = R_L\left(\frac{V_{in}}{V_Z} - 1\right)$

$$= 400\left[\frac{9}{5} - 1\right].$$

$$= 320\Omega$$

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$$R_{S\,min} = \frac{V_{in}V_Z - V_Z^2}{P_{Z\,max}}$$

$$= \frac{(9 \times 5) - 25}{0.5} = 40\Omega$$

Suitable value of R_s would be.
$40\Omega - 320\Omega$

→ O/P Resistance and Voltage Regulation

In a perfect power supply O/P voltage would remain constant regardless of current taken by the load. However O/P voltage falls as load current increases.

So ideally power supply should have zero internal resistance

This internal resistance appears at the O/P of supply. It is defined as ratio of change in O/P voltage to change in O/P current.

$$R_o = \frac{\text{change in O/P vtg}}{\text{change in O/P current}} = \frac{dV_o}{dI_L}$$

dV_o - Small change in O/P voltage
dI_L - Small change in O/P current.

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→ Regulation of power Supply :-

Regulation of power supply is

$$\text{regulation} = \frac{\text{change in o/p vtg}}{\text{change in i/p vtg}} \times 100.$$

Ideally value of regulation should be very small.

Simple Zener diode regulators have values of regulation 5% to 10%.

→ The following data were obtained during a test carried out on a dd power supply

Load test
- o/p vtg (no-load) = 12V.
- o/p vtg (2A load current) = 11.5V.

Regulation test
- o/p vtg (mains i/p 220V) = 12V.
- o/p vtg (mains i/p 200V) = 11.9V.

Determine equivalent o/p resistance of power supply.

Regulation of power supply

Sol:- $R_o = \frac{\text{change in o/p vtg}}{\text{change in o/p current}}$

$= \frac{12 - 11.5}{2 - 0} = \frac{0.5}{2} = 0.25\ \Omega$

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Regulation = $\frac{\text{change in o/p volt}}{\text{change in i/p volt}} \times 100$.

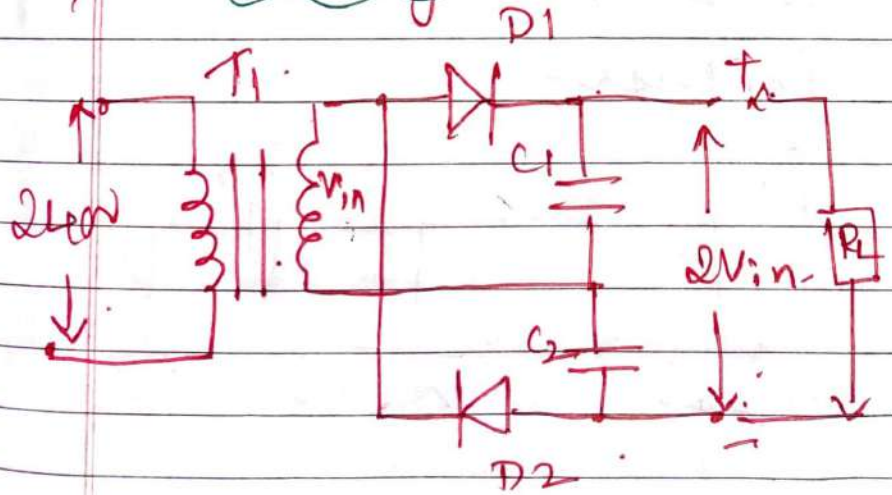
$= \frac{12 - 11.9}{220 - 200} \times 100$

$= 0.5\%$.

→ **Voltage Multipliers :-**

Voltage multiplier is a modified capacitor filter that delivers a dc voltage twice or ~~three~~ more times of peak value of the i/p ac volt. Such power supplies are used in cathode ray tubes (picture tube in TV receivers oscilloscopes and computer display).

→ **Voltage Doubler :-**



The circuit diagram for full wave voltage doubler is as shown.

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Initially all capacitors stored 0V.

During +ve half cycle of I/P signal V_{in}, D_1 is forward biased conducts, charges the capacitor C_1 to peak v.tg of V_{peak}. & D_2 is reverse biased.

During -ve half cycle of I/P signal V_{in} D_2 is forward biased & charges capacitor C_2 to peak v.tg.

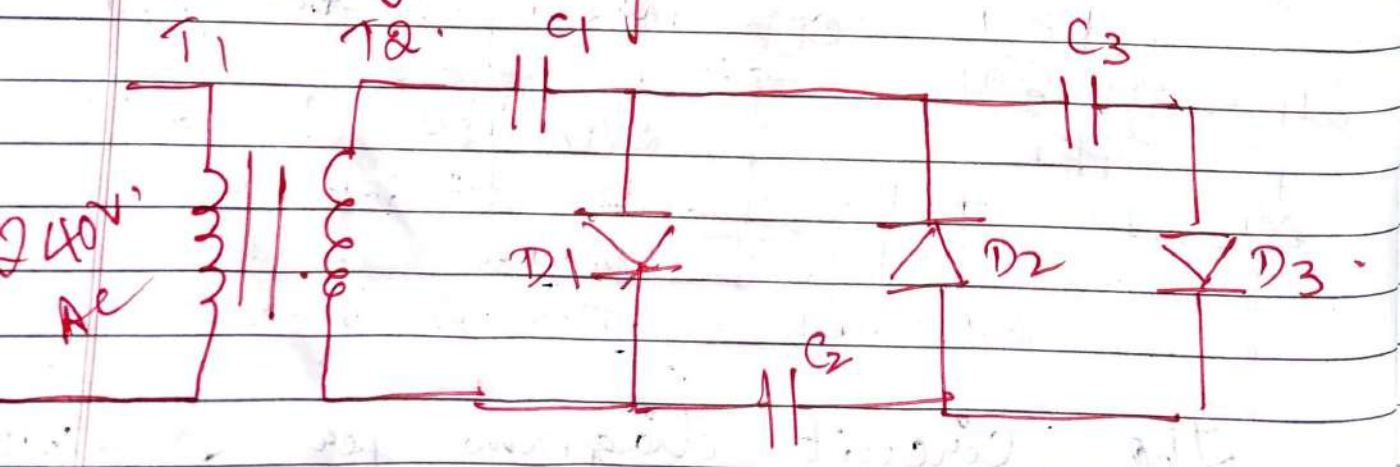
The O/P v.tg will be equal to total voltages across C_1 and C_2.

$$V_{out} = V_{peak} + V_{peak} = 2V_{peak}.$$

Note: If diodes are not ideal than O/P will be $2V_{peak}$ − drop across diodes.

⇒ ~~Voltage Doubler~~:

⇒ Voltage Tripler:



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The voltage tripler produces 3 times the i/p vtg.

Assume all capacitors store 0 v.

During +ve half cycle, D1 conducts and C_1 gets charged to V_{in}. $C1 = V_{in}$

During -ve half cycle, D2 is forward biased and D1 is reverse biased. C_2 gets charged with voltage of $C_1 (V_{in})$.

So $C_2 = 2V_{in}$.

During second positive half cycle diode D1 and D3 conducts. D2 is RB. C_2 charges C_3 upto $2V_{in}$. Across C_1 it is V_{in}.

So total vtg $V_{in} + 2V_{in} = 3V_{in}$

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→ **Amplifiers:**

Amplifier is an electronic circuit which increases the amplitude of its i/p signal without changing other parameters.

→ **Types of Amplifiers:**

→ **AC Coupled Amplifiers:-**

Stages are coupled in such a way that DC levels are blocked and only AC components are transferred from stage to stage.

→ **DC Coupled Amplifiers:-**

In DC or Direct coupled both ac and dc components are transferred from stage to stage.

→ **Large Signal Amplifiers:-**

Designed for large signal 10 - 100V.

→ **Small Signal Amplifiers:-**

Designed for low-level signals

less than 1V.

→ **Audio freq Amplifiers:-**

operate in band of freq's 20Hz - 20kHz.

→ **Wide Band Amplifiers:-**

Amplify signals over wide range of freq's few tens to Megahertz.

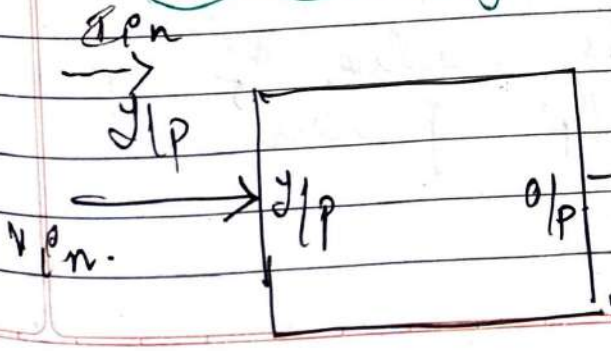
→ **Radio freq Amplifiers:-**

operate in band of freq's 100kHz to 1GHz

→ **Low noise Amplifiers:-**

Designed so that they contribute negligible noise. Operate with small signal levels less than 1mV.

→ **Block Diagram of an Amplifier:-**



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Block diagram of amplifier showing i/p and o/p voltages and currents.

→ Amplifier parameters :-

Gain :- Gain is the amount of amplification. It can be v/g gain, current gain or power gain.

In general Gain is ratio of output and i/p. represented by A.

Voltage gain is ratio of o/p v/g to i/p v/g.

$$A_V = \frac{V_o}{V_{in}}$$

Current gain is ratio of o/p current to i/p current.

$$A_I = \frac{I_{out}}{I_{in}}$$

Power gain is ratio of o/p power to i/p power

$$A_P = \frac{P_{out}}{P_{in}}$$

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Power is product of current and vtg $P = IV$

$$A_p = \frac{P_{out}}{P_{in}} = \frac{I_{out} V_{out}}{I_{in} V_{in}}$$

$$= \frac{I_{out}}{I_{in}} \times \frac{V_{out}}{V_{in}}$$

$$\boxed{A_p = A_I \times A_V}$$

Example: An amplifier produces an o/p vtg of 2V for an i/p of 50mV. If i/p and o/p currents are 4mA and 200mA respectively. Find
vtg gain
current gain
power gain.

$$A_V = \frac{V_o}{V_{in}} = \frac{2}{50mV} = 40.$$

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Current gain $A_I = \frac{I_{out}}{I_{in}} = \frac{200\,mA}{4\,mA}$

$A_I = 50$

power gain = $A_I \times A_V = 40 \times 50$

$= 2000$

→ Input Resistance (Rin) :- It is defined as ratio of i/p v.tg to i/p current. Expressed in Ω.

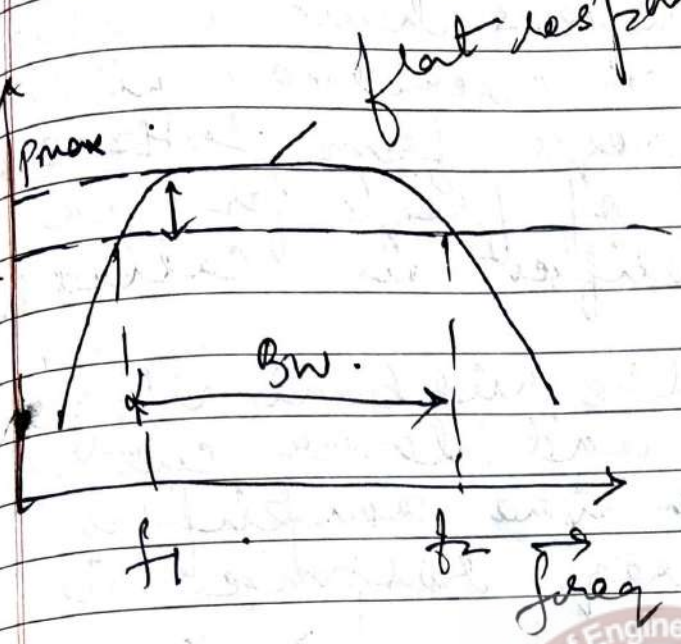
→ O/p. Resistance (Ro) It is defined as ratio of o/p v.tg to o/p current. measured in Ω.

→ Freq Response: It is the graph plotted for gain versus i/p freq. The freq response is measured in terms of upper (f_2) & lower (f_1) cut off freq's of the amplifier.

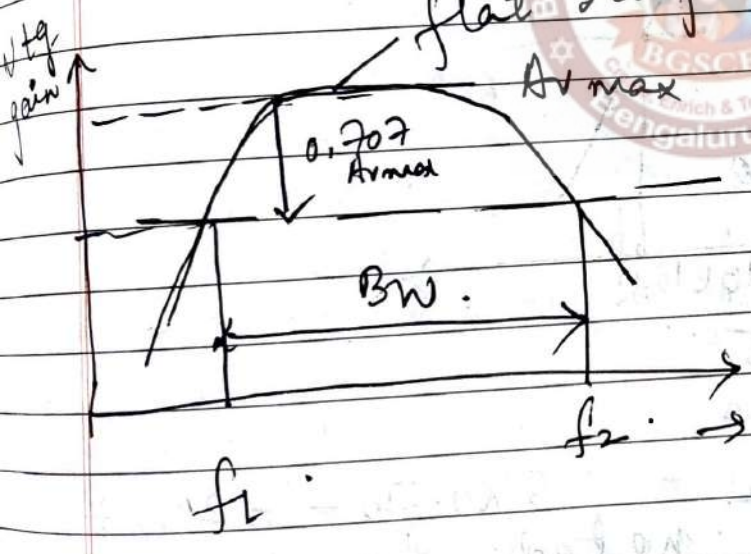
These freq's are calculated as follows:

O/p power dropped to 50% or v.tg gain dropped to 70.7%.

of its mid value.



O/p power V/s freq.



→ Bandwidth: (BW) of an amplifier is difference between upper and lower cut off freq's. $(f_2 - f_1)$.

The range of freq's within a band is known as BW.

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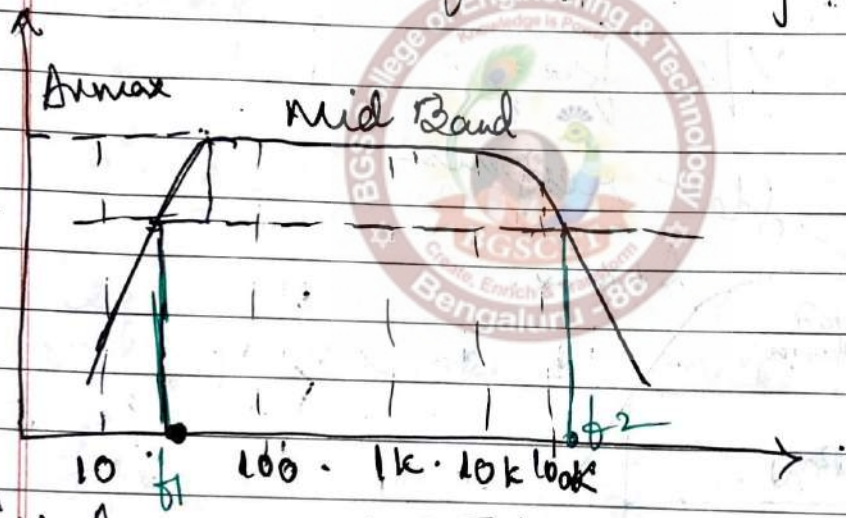
Example:

Audio amplifiers have a flat freq response over the audio range of freq's from 20Hz - 20kHz. This range of freq's for an audio amplifier is called Bw.

Determine the mid band vtg gain and upper and lower cut off freq's for the amplifier whose freq response is.



Sol^{n}: Avmax = 35.

0.707 x Avmax = 35 x 0.707 = 24.7.

f1 & f2 are noted down.

Bw = f2 - f1.

→ Phase Shift:

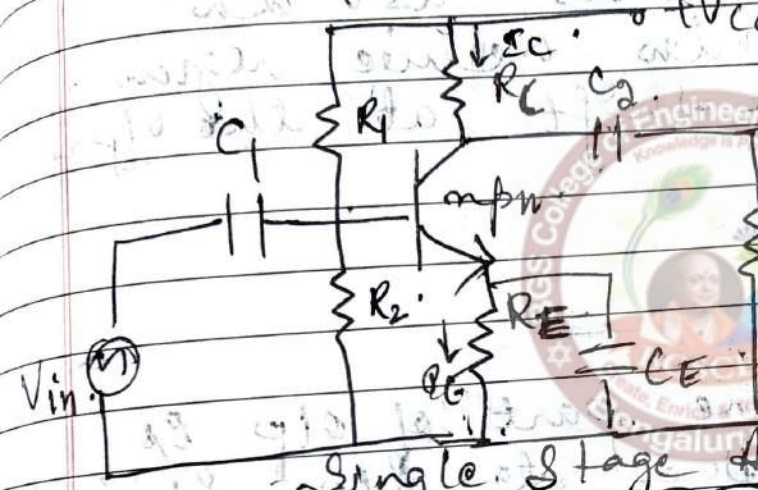
Phase shift is phase angle betw the i/p and o/p vtg.

measured in degrees.

Measurement is carried out in mid band.

Conventional Single Stage transistor amplifier provide phase shifts of 180° or 360°.

Transistor As an Amplifier:



Single Stage Amplifier

Transistor is connected in Common emitter configuration.

C_1 Couples i/p to base of transistor

C_2 Couples o/p from collector to load.

C_E - emitter bypass capacitor provides low reactance path.

R_1, R_2 R_E & R_C provide biasing to make transistor operate in active region.

The flow of current I_C through collector

When ac i/p signal is given to base of transistor

emitter base junction is forward biased & collector base junction is reverse biased.

Hence there is flow of emitter current I_E, base current I_B & o/p current I_C.

As large I_E flows through R_C, it results in large o/p at the load.

So o/p is amplified.

Transistor works as an amplifier in active region.

The phase shift at the o/p is 180°.

→ Feed Back:

If o/p some part of o/p is connected back to i/p, it is called feed back.

If o/p is not connected to i/p then it is called open loop system.

If there is feed back then it is called Closed loop system.

2 types of feedback

→ positive - flb

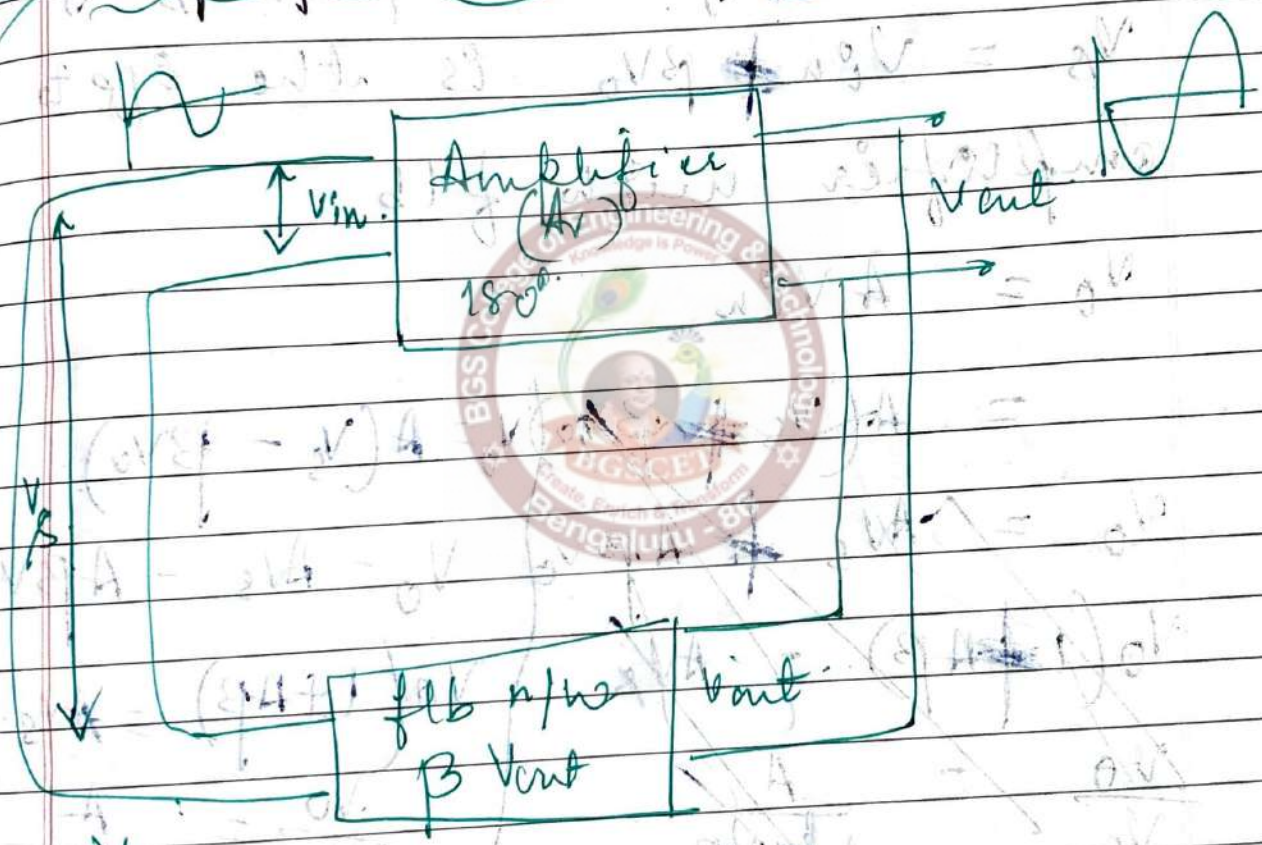
→ negative - flb

positive flb: o/p is fed back in such a way so as to

reinforce the i/p.

negative flb:- o/p is fed back to i/p such a way so as to subtract from it.

→ Amplifier with feedback:-



$V_f = \beta V_o$

V_{in} is the o/p to amplifier
V_o is the o/p with a phase shift of 180°. This o/p V_o is fed back to i/p of amplifier through flb network.
V_f is the o/p of flb network

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$V_f = \beta V_o$.

Gain of amplifier without fb is $A = \frac{V_o}{V_{in}}$

$V_o = A V_{in}$

Now $V_{in} + V_f = V_s$. $\quad V_{in} = V_s - V_f$

$V_s = V_{in} + \beta V_o$ is the o/p to amplifier with fb.

$V_o = A V_{in}$

$= A(V_s + \beta V_o)$ $\quad V_o = A(V_s - \beta V_o)$

$V_o = A V_s + A\beta V_o$ $\quad V_o = A V_s - A\beta V_o$

$V_o(1 + A\beta) = A V_s$ $\quad V_o(1 + A\beta) = A V_s$

$\frac{V_o}{V_s} = \frac{A}{1 + A\beta}$ $\quad \frac{V_o}{V_s} = \frac{A}{1 + A\beta}$

$\frac{V_o}{V_s}$ is gain of amplifier with fb.

$$\frac{V_o}{V_s} = A_f = \frac{A}{1 + A\beta}$$

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A is open loop gain of amplifier.
β is f/b factor.

Example:

→ An amplifier with negative feedback applied has open loop gain of 50. & one-tenth of its o/p is fed back to i/p (β=0.1). Determine overall v/g gain with negative f/b applied.

Sol: $A_f = \frac{A}{1+A\beta} = \frac{50}{1+50\times0.1} = 8.33$

→ In above ex amplifier open loop v/g gain increases by 20%. Determine the % decrease in overall v/g gain.

Sol: new v/g gain is

$A_2 = A_0 + 0.2A_0$
$= 50 + 0.2(50) = 60$

& v/g gain with -ve f/b.

$\frac{A_0}{1+A_f\beta} = \frac{60}{1+60(0.1)} = 8.57$

% increase in V to gain

$$\% = \frac{8.57 - 8.33}{8.33} \times 100$$

$$= 2.88\%$$

→ An Integrated ckt that produces an open-loop gain of 100 to be used as basis of an amplifier having a precise V/g gain of 20. Determine amount of feedback reqd.

$A_f = \frac{A_v}{1+\beta A_v}$ = closed loop gain.

$A_v = 100$

$A_f = 20$

$\beta = \frac{1}{A_f} - \frac{1}{A_v}$

$= 0.05 - 0.01$

$\boxed{\beta = 0.04}$

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Multistage Amplifiers:

In order to provide sufficiently large values of gain number of interconnected stages are connected within an amplifier.

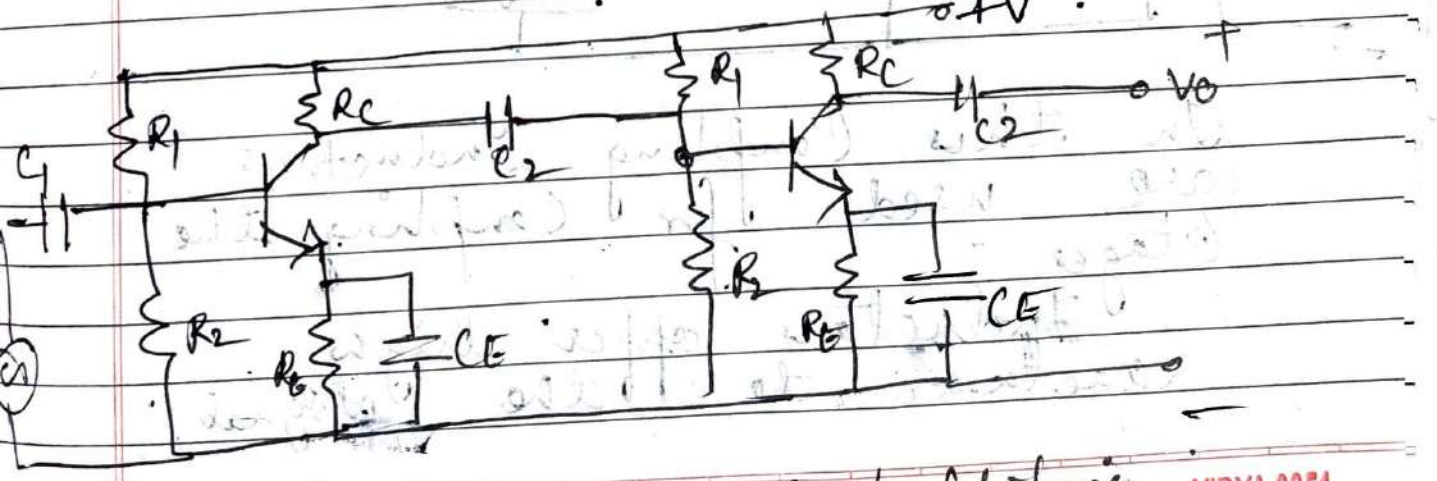
O/p of first stage is connected to i/p of second stage through a suitable coupling.

A_{V_1} A_{V_2} A_{V_3}.

Overall gain is product of individual stage gain

$A_V = A_{V_1} \times A_{V_2} \times A_{V_3}$.

When gain increases BW reduces. BW of multistage will be less than individual stage BW.



2-stage RC coupled amplifier

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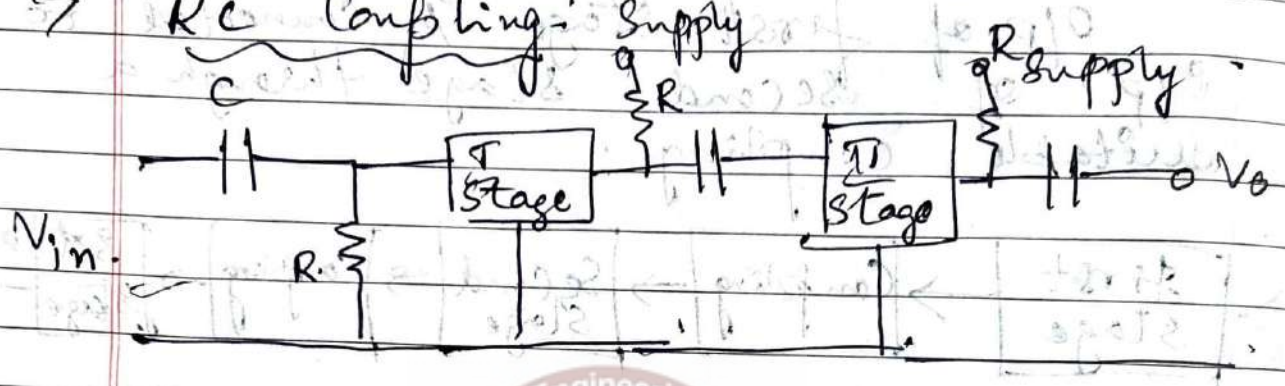
Different Types of Coupling:-

Signals can be coupled between individual stages of multistage amplifier.

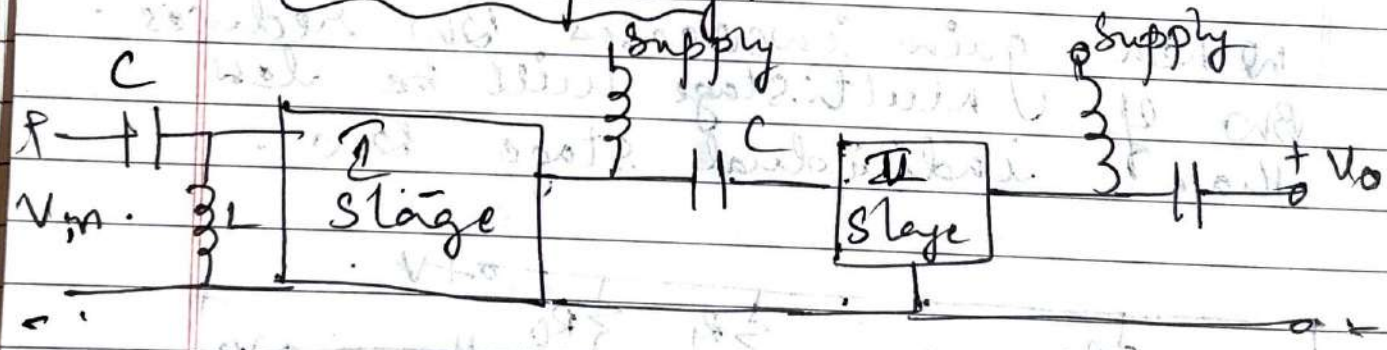
→ **RC Coupling:-**



In this coupling method stages are coupled together using capacitors and resistors.

Capacitors provide low reactance to the signal.

→ **L-C Coupling:**



In this coupling Inductors are used for coupling the stages.

Inductors offer high reactance to the signal.

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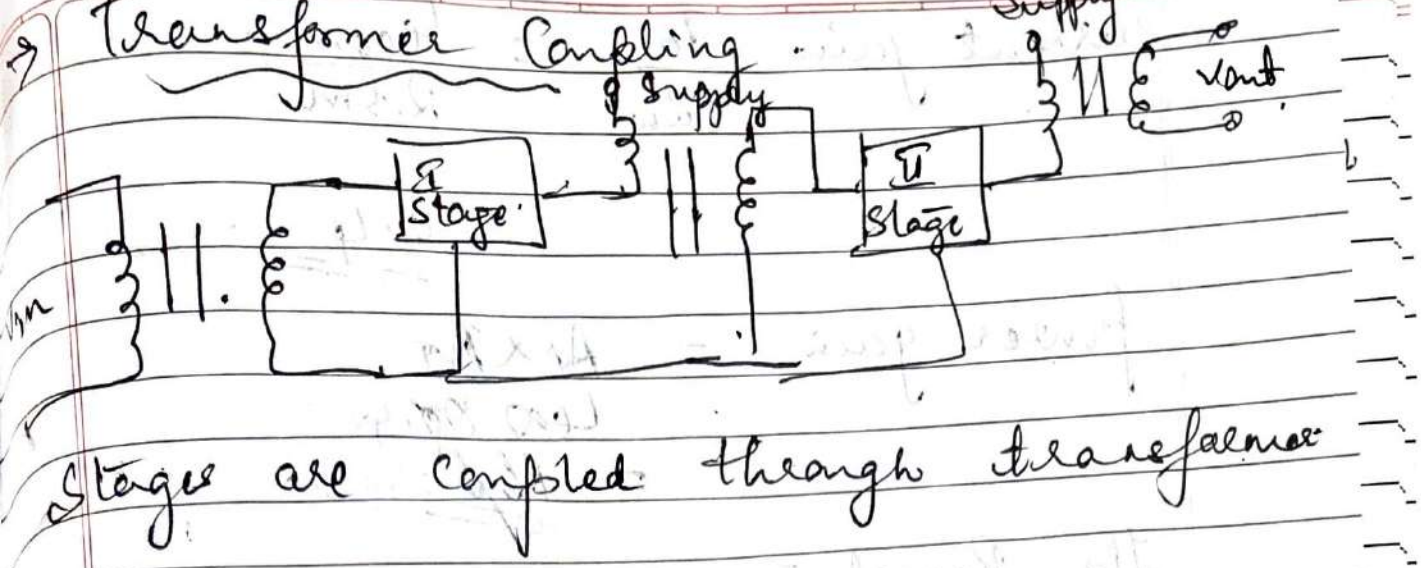
Transformer Coupling.



Stages are coupled through transformer

Direct Coupling:

Stages are coupled only using resistance

Problems:

The following measurements are made during test on an amplifier.

$V_{in} = 250mV$, $I_{in} = 2.5mA$, $V_{out} = 10V$.
$I_{out} = 400mA$.
Find vtg gain, current gain, power gain, I/p resistance.

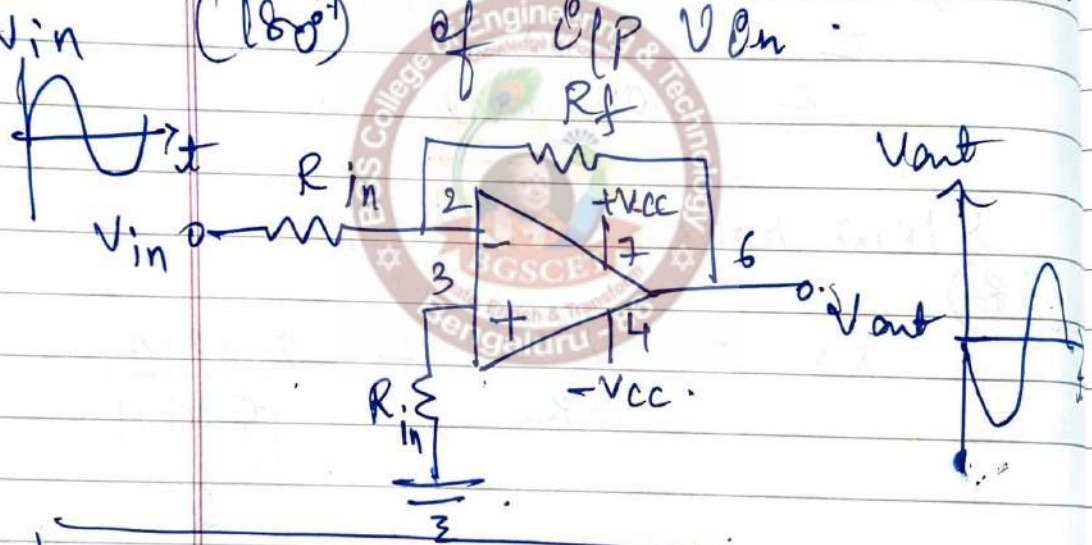
Vtg gain $A_v = \frac{V_{out}}{V_{in}} = \frac{10}{250m} = 4000$.

→ Op Amp Configuration / Opamp circuits :-

→ Inverting op-amp :-

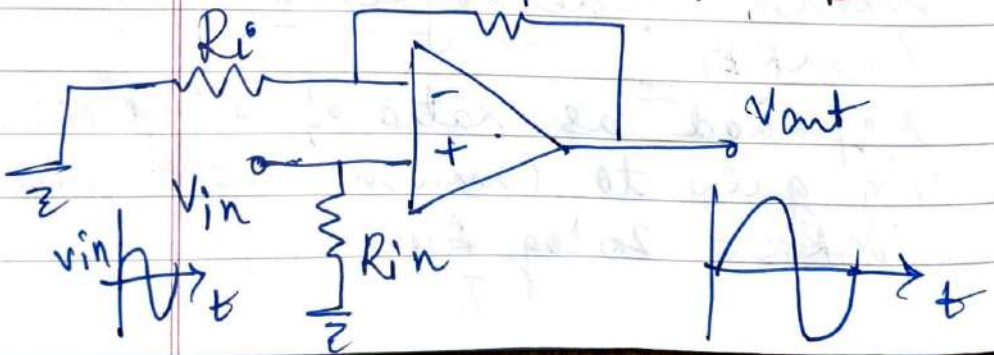
I/p Vin is applied to inverting terminal of opamp and non-inverting terminal is grounded.

O/p is inverted version (180°) of I/p Vin.



$$Vout = -Vin\left(\frac{Rf}{Rin}\right).$$

→ Non-Inverting opamp :-



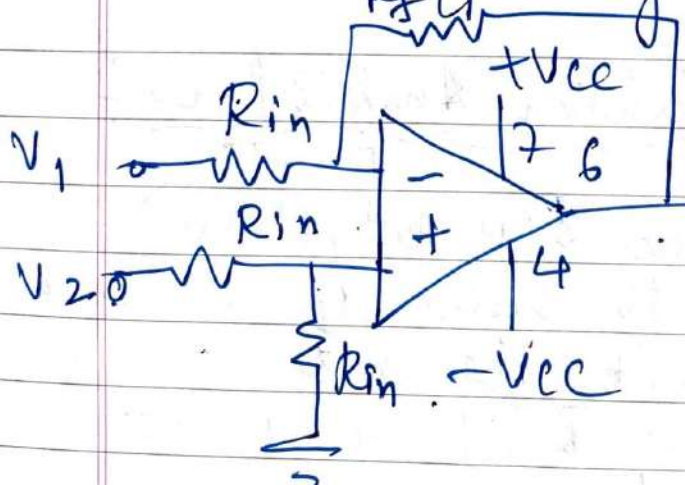
I/p signal V_{in} is applied to non-inverting terminal of an opamp. Inverting terminal is grounded. O/p is amplified and phase shift.

$$V_o = V_{in}\left[1 + \frac{R_f}{R_{in}}\right]$$

→ Differential Amplifier:

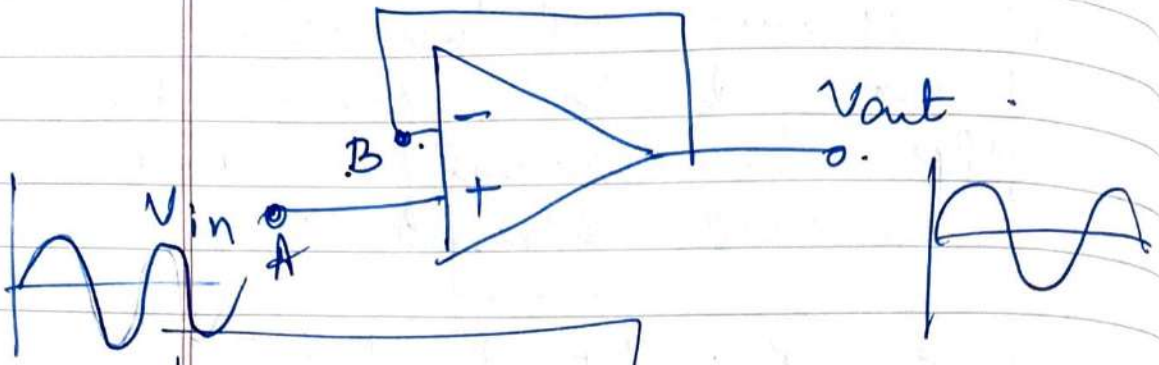
I/p is given to both the terminals of opamp.

O/p is amplified version of difference between two I/p signals V_1 and V_2.



$$V_{out} = V_2 - V_1.$$

→ Voltage follower opamp:-



$V_{out} = V_{in}$

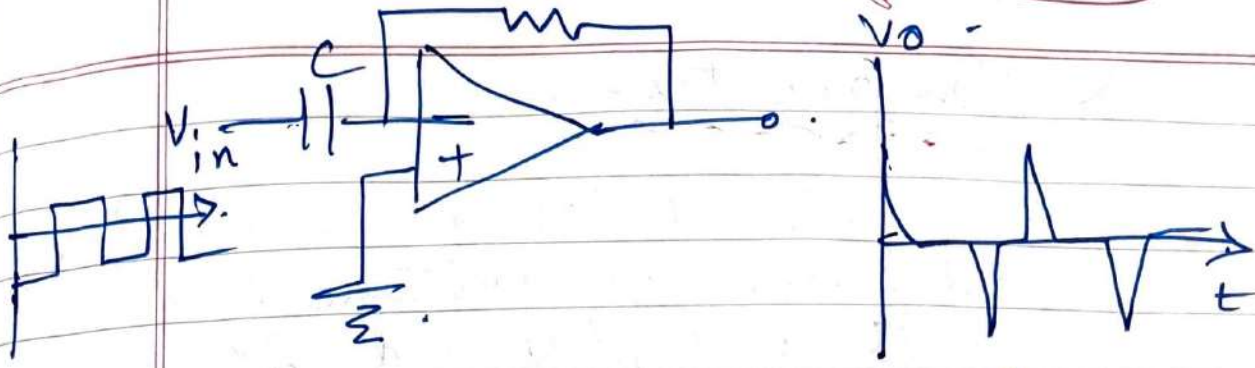
o/p vtg follows the i/p. So it is called as vtg follower. o/p is connected back to i/p so that feedback is 100%

→ Properties of voltage follower:

Voltage gain = 1.
i/p Impedance $R_{in} = \infty$.
o/p Impedance $R_{out} = 0$.

→ Differentiater Amplifier:-

It produces o/p vtg (Vout) proportional to rate of change of i/p V_{in}. It is an inverting amplifier that uses capacitor.

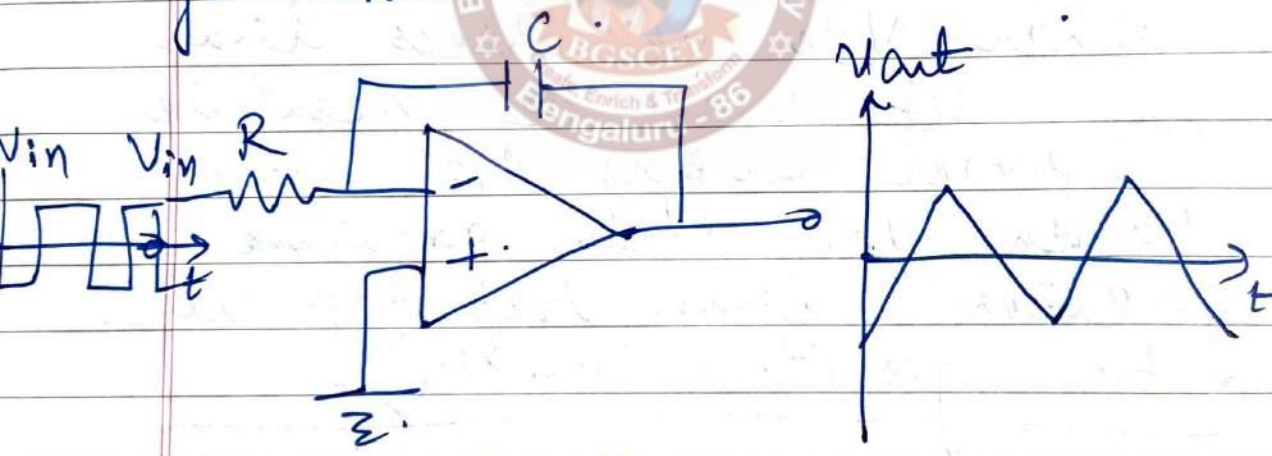


for a square wave i/p o/p is pulses.

$$V_{out} = -RC \frac{dV_{in}}{dt}$$

→ Integrator Amplifier:-

It produces an o/p v tg proportional to integral of i/p v tg V_{in}

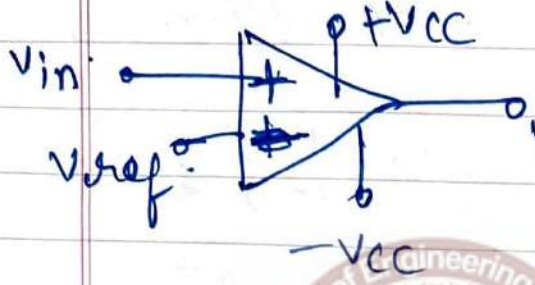


It uses R in series with V_{in}. Capacitor is connected in feedback.

$$V_o = -\frac{1}{RC} \int_0^t V_{in}\, dt$$

→ Comparater:-

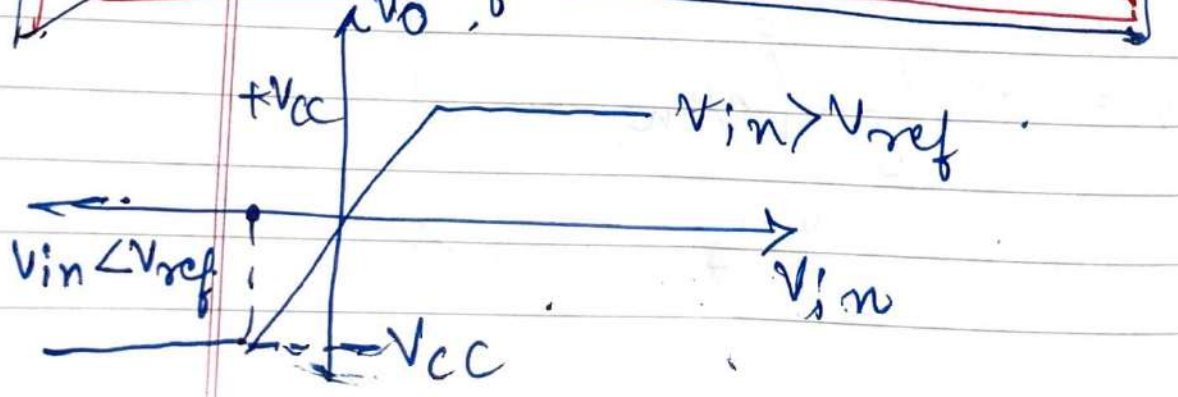
opamp voltage comparator compares magnitude of two voltages i/p's and determines which is larger of the two.



opamp is given two i/ps V_{in} and V_{ref}.
When V_{in} is less than V_{ref} o/p will be negative power supply i.e $-V_{cc}$.
When V_{in} is greater than V_{ref} o/p will be positive $(+V_{cc})$.

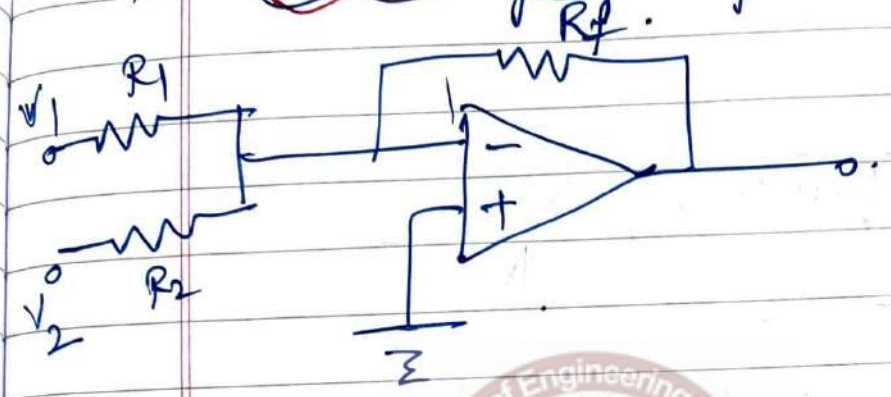
$V_{in} < V_{ref}$ $V_o = -V_{cc}$

$V_{in} > V_{ref}$ $V_o = +V_{cc}$.



opamp comparator is a device whose o/p is dependent on value of i/p voltages.

→ Summing opamp:-



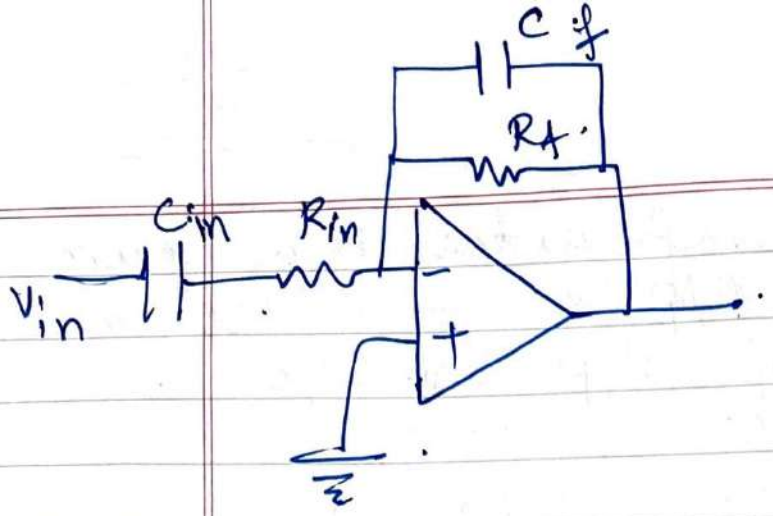
The summer circuit is as shown. I/p's are given to inverting terminal.

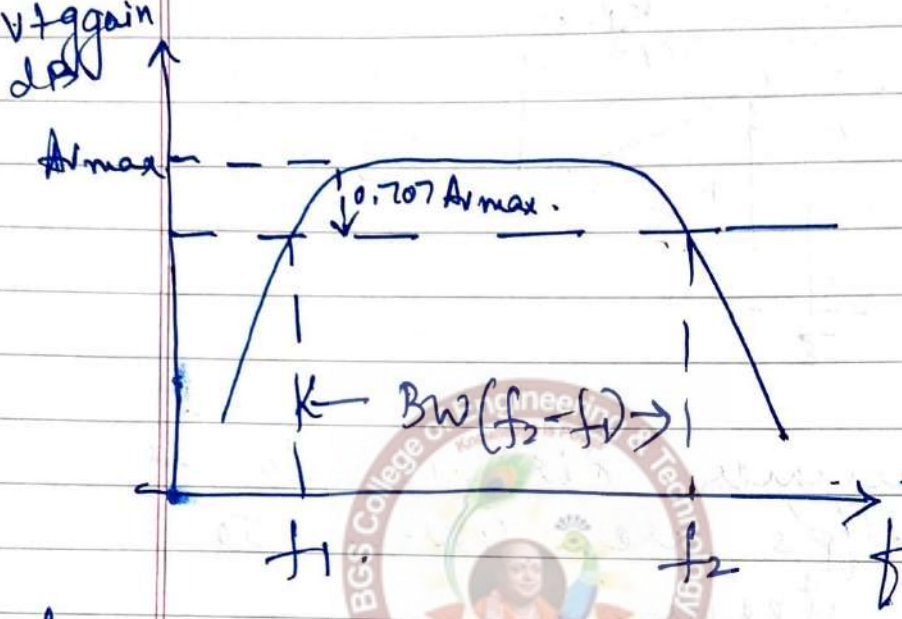
o/p vtg is proportional to algebraic sum of i/p vtgs V_1 and V_2.

$$V_{out} = -(V_1 + V_2)$$

→ Effect of i/p and feedback capacitors

By selecting appropriate values of capacitor freq response of inverting opamp may be easily modified.





Lower cut off freq is determined by i/p capacitor Cin & Rin.

$$f_1 = \frac{1}{2\pi R_{in} C_{in}} = \frac{0.159}{R_{in} C_{in}}$$

Upper cut off freq is determined by o/p f1b capacitor Cf and f1b resistor Rf

$$f_2 = \frac{1}{2\pi R_f C_f} = \frac{0.159}{R_f C_f}$$

→ With no fb applied opamp produces an o/p of 10V from a differential amplifier o/p of 50μV. With the i/p's shorted together same opamp produces an o/p of 500mV when an i/p of 2V is present. Determine value of Common-mode rejection mode.

Soln:- $CMRR = \frac{A_{V(D)}}{A_{V(C)}}$

$A_{V(D)} = \frac{V_{O(D)}}{V_{in}} = \frac{10}{50\mu} = 200000.$

$A_{V(C)} = \frac{V_{O(C)}}{V_{in(C)}} = \frac{500m}{2V} = 0.25$

$CMRR = 20 \log\left(\frac{200000}{0.25}\right)$

$= 118dB.$

→ An inverting amplifier is to operate according to following specifications.

Voltage gain = 100.
I/P resistance = 10kΩ.
Lower cut off freq = 250Hz.
Upper cut off freq = 15kHz.
Device a circuit to satisfy above specifications using an opamp.

Sol^n :- $R_{in} = 10k\Omega$.

$$A_v = \frac{R_f}{R_1}$$

$$R_f = A_v \times R_1 = 100 \times 10k$$
$$= 1000k\Omega$$

To find C_{in}

$$f_1 = \frac{0.159}{R_{in} C_{in}}$$

$$C_{in} = \frac{0.159}{250 \times 10k}$$

$$C_{in} = 63nF$$

$$f_2 = \frac{0.159}{R_f C_f}$$

$$C_f = \frac{0.159}{15 \times 10^3 \times 1000 \times 10^3}$$

$$C_f = \frac{0.159 \times 10^{-6}}{15000}$$

$$= 1.06 \times 10^{-11} \text{ F}$$

→ An opamp has an open loop gain of 100 dB. If inverting i/p is held at 0V & non inverting i/p is connected to v.tg source of 0.1mV. find the o/p v.tg

$$A_V(\text{dB}) = 20 \log \frac{V_o}{V_{in}}$$

$$100 = 20 \log \frac{V_o}{0.1m}$$

$$5 = \log \frac{V_o}{0.1m}$$

$$100000 = \frac{V_o}{0.1 \times 10^{-3}}$$

$$10000 \times 10^{-3} = V_o$$

$$V_o = 10 \text{ V}$$

→ An Inverting opamp is reqd to have a V$_{cl}$ gain 40 and an i/p resistance of 5kΩ. Determine the value of fb resistance.

$A_v = 40$

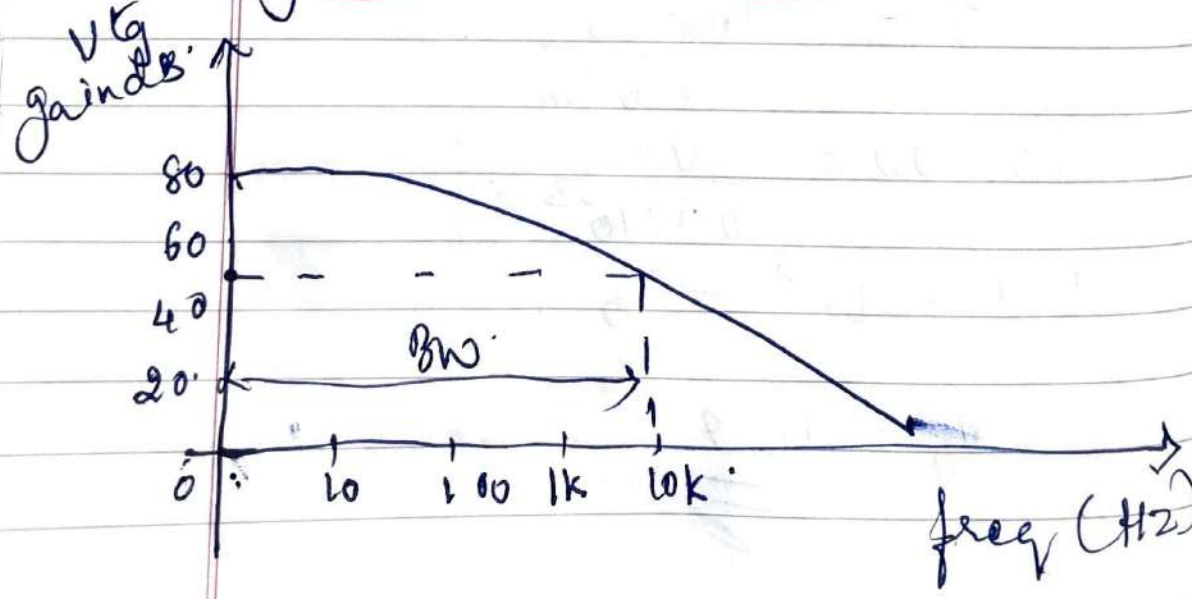
$R_{in} = 5k\Omega$

$A_v = \frac{R_f}{R_{in}}$

$40 = \frac{R_f}{5k}$

$R_f = 200k\Omega$

→ The open loop freq response of an opamp is shown. Determine the bandwidth of amplifier if closed loop gain is 46dB.



from the fig BW = 10k

→ An opamp has an open loop vtg gain of 100dB. If the inverting i/p held at 0V and non inverting i/p is connected to i/p of 0.2mV. find the o/p vtg.

Sol:-

$$\text{Gain} = 20\log\frac{V_o}{V_{in}}$$

$$100 = 20\log\frac{V_o}{0.2\times10^{-3}}$$

$$5 = \log\frac{V_o}{0.2\times10^{-3}}$$

$$100000 = \frac{V_o}{0.2\times10^{-3}}$$

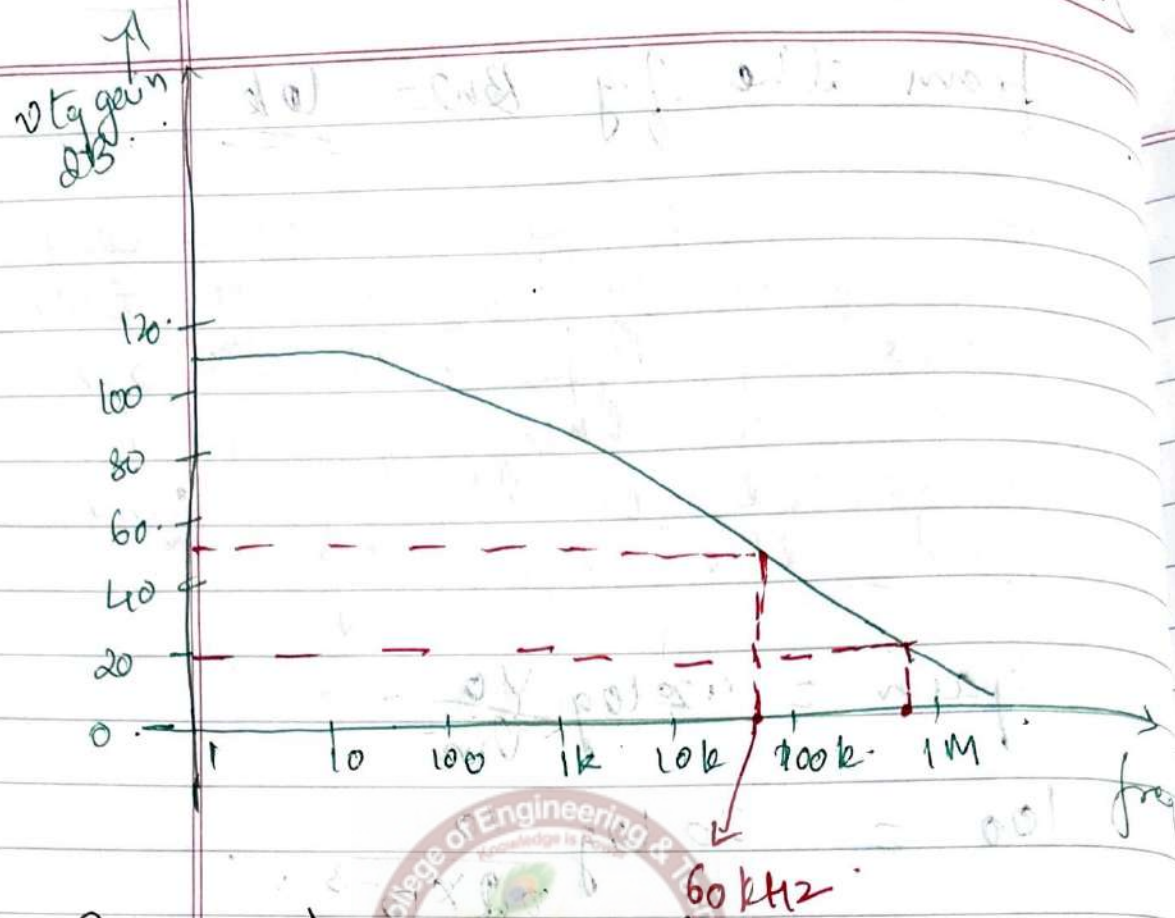
$$V_o = 20000 \times 10^{-3}$$

$$V_o = 20V$$

→ The open loop freq response of an opamp is as shown. Determine

→ vtg gain for a BW of 60kHz

→ BW for a vtg gain of 20dB.

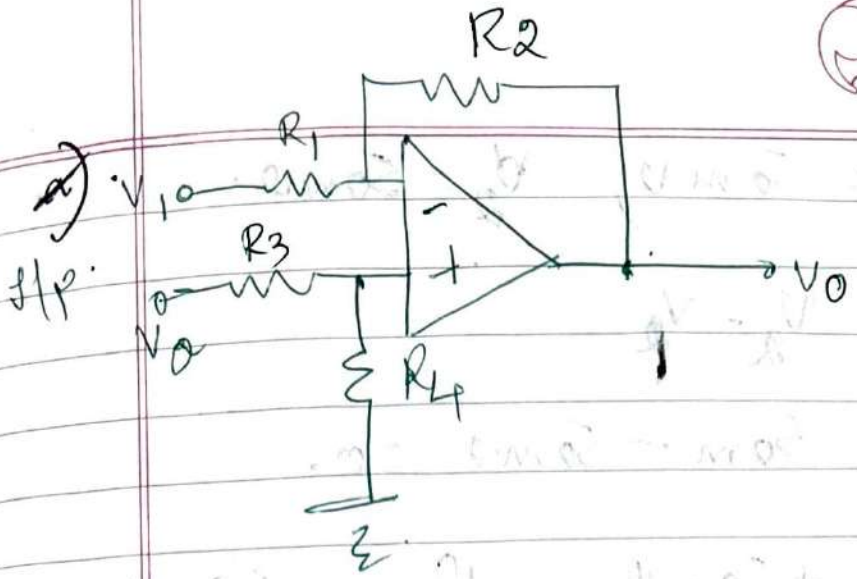


a) Gain for 60 kHz is 50dB.
b) Bw for gain of 20dB is 900KHz

→ An opamp i/p connected in differential mode as shown. If $R_2 = R_4 = 20k\Omega$, $R_1 = R_3 = 1k\Omega$ determine the o/p vtg for the following:

	V_1	V_2
a	0	50mV
b	50mV	0.
c	+50m	+50m
d	+50mV	-50mV.
e	-50mV.	+50mV.
f	-50mV	-50mV.

a)



(a) $V_1 = 0V, \quad V_2 = 50mV.$

$$\text{Gain} = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$$

$$\frac{V_o}{50m} = 1 + \frac{20k}{1k}$$

$$V_o = 50m \times 21$$

$$V_o = 1.05V \quad 1.05V$$

(b) $V_1 = 50mV, \quad V_2 = 0.$

$$\text{Gain} = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

$$\frac{V_o}{50m} = \frac{-20k}{1k}$$

$$V_o = -1.05V \quad -1V$$

$$V_o = -1V$$

(c). $v_1 = 50mv$, $v_2 = 50mv$.

$v_0 = v_2 - v_1$

$= 50m - 50mv = 0$.

(d). $v_1 = +50mv$, $v_2 = -50mv$.

$v_0 = v_2 - v_1$

$= -50m - (+50mv)$

$= -2mv$. $-100mv$.

(e). $v_1 = -50mv$, $v_2 = 50mv$

$v_0 = v_2 - v_1$

$= 50m - (-50mv)$

$= 2mv$. $100mv$.

(f) $v_1 = -50mv$, $v_2 = -50mv$.

$v_0 = v_2 - v_1$

$= -50m - (-50m)$

$= 0v$.

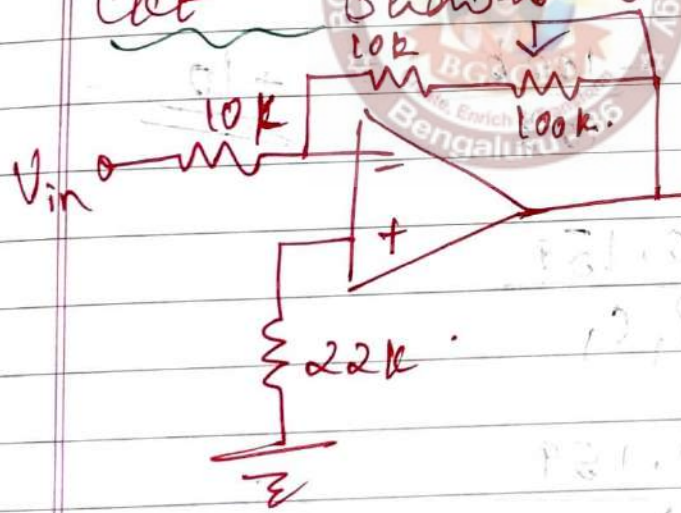
→ An opamp has gain BW product of 2×10^5. Estimate the BW of the device if closed loop gain is

a) 50
b) 2000.

(a) Gain x BW = 2×10^5.
So x BW = 2×10^5
BW = 4 kHz.

(b) Gain x BW = ~~2000~~ 2×10^5.
2000 x BW = 2×10^5
BW = 100 Hz.

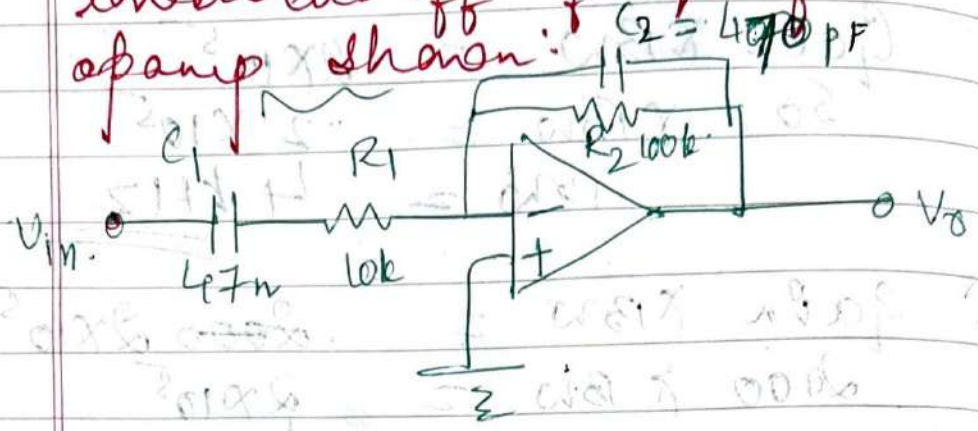
→ Determine the maximum and minimum o/p gain for the ckt shown.



Sol^n. ckt is inverting opamp.
So gain = $-\frac{R_f}{R_1}$

Max R_f = 100k + 10k = 110k.
Min R_f = 10k.
Max Gain = $-\frac{110k}{10k} = -11$
Min Gain = $-\frac{10k}{10k} = -1$.

→ Determine the mid-band v/g gain and upper and lower cut off freq's for opamp shown:



Sol^n: Mid band v/g gain

$$A_v = \frac{+R_2}{R_1}$$

$$= \frac{+100k}{10k} = \underline{\underline{+10}}$$

$$f_1 = \frac{0.159}{R_1 C_1}$$

$$= \frac{0.159}{10k \times 47 \times 10^{-9}}$$

$$= \frac{0.159}{470 \times 10^{-6}}$$

$$= 3.38 \times 10^{2}$$

$$= \underline{\underline{338\ Hz}}$$

$$f_2 = \frac{0.159}{R_f C_f}$$

$$f_2 = \frac{0.159}{100 \times 470 \times 10^{-9}}$$

$$= 3.38 \times 10^{3}.$$

$$= 3.38 \text{ kHz}$$

→ An audio amplifier is to operate according to following specification

Dtg gain = 50. A_V.

I/p resistance = 5kΩ R_1

f_1 Lower cut off freq = 10 Hz

f_2 upper cut " " = 20 kHz.

Devise a circuit to satisfy the above specification using an op-amp.

$$A_V = \frac{R_f}{R_1} \qquad A_V = \frac{R_2}{R_1}.$$

$$50 = \frac{R_f}{5k} \qquad 50 = \frac{R_2}{5k}.$$

$$R_2 = 250 \text{ kΩ}.$$

$$C_1 = \frac{0.159}{R_1 f_1}$$

$$C_1 = \frac{0.159}{5k \times 10.}$$

$$C_1 = 3.18\ \mu F.$$

$$C_2 \text{ or } C_f = \frac{0.159}{R_2 f_2.}$$

$$= \frac{0.159}{250k \times 20k.}$$

$$= \frac{0.159}{5 \times 10^6}$$

$$C_2 = 0.0318\ \mu F.$$

Module - 2.

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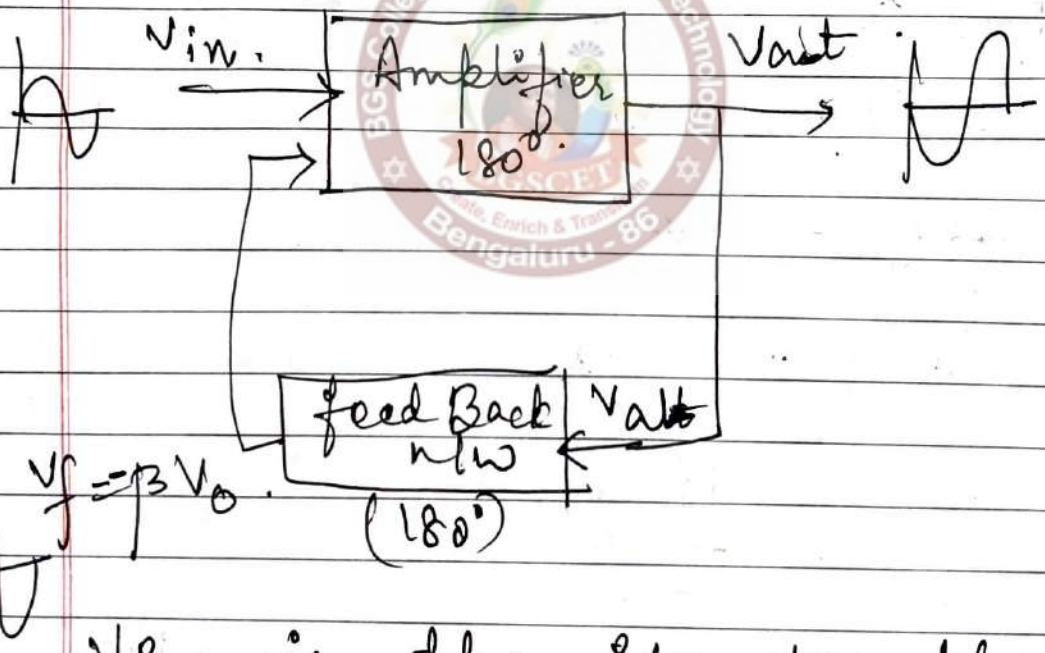
Oscillators :-

Oscillators are circuits that generate sine wave, square wave, triangular waveforms.

Positive feedback is applied in oscillators.

Oscillators consists of amplifier and feedback network.

Block diagram of Oscillators :-



$V_f = \beta V_o$.

V_{in} is the i/p to the amplifier. V_o is the o/p. amplified and shifted in phase by 180°.

open loop vtg gain

$$A_v = \frac{V_o}{V_{in}}$$

The o/p V_o is fed back to

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V_f through feedback network.

The feedback network provides a phase shift of 180°. O/p of feedback n/w $V_f = -\beta V_o$ '-' because 180° phase shift.

V_f and V_{in} are in phase, so oscillators uses +ve f/b.

$V_s = V_{in} + V_f$ is the total i/p to amplifier.

$V_s = V_{in} - \beta V_o$. so $V_{in} = V_s + \beta V_o$.

$V_o = A_V V_{in}$

$V_o = A_V(V_s + \beta V_o)$

$V_o - A_V\beta V_o = A_V V_s$

$V_o(1 - A_V\beta) = A_V V_s$

$\frac{V_o}{V_s} = \frac{A_V}{1 - A_V\beta}$.

$\boxed{A_f = \frac{A_V}{1 - A_V\beta}}$ is closed loop v/g gain with +ve f/b.

→ Sinusoidal oscillators : produce sine wave

Non-sinusoidal oscillators : produce square/rectangular wave.

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→ Illustration of effect of -ve and +ve flb on overall v/g gain :-

Case 1 Assume amplifier with gain of 9 and one-tenth of o/p is fed back to i/p.

$A_v = 9$

$\beta = 0.1$.

loop gain $A_v\beta = 0.9$.

over all gain with -ve flb.

$$\frac{A_v}{1+A_v\beta} = \frac{9}{1+0.9} = \frac{9}{1.9} = 4.7$$

With +ve flb over all v/g gain.

$$\frac{A_v}{1-A_v\beta} = \frac{9}{1-0.9} = 90$$

Case 2: Assume amplifier with gain of 10 and one-tenth of o/p is fed back to i/p.

$A_v = 10$. $\beta = 0.1$.

loop gain $A_v\beta = 1$.

Gain with -ve flb.

$$\frac{A_v}{1+A_v\beta} = \frac{10}{1+1} = 5$$

Gain with +ve flb.

$$\frac{A_v}{1-A_v\beta} = \frac{10}{1-1} = \infty$$

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This shows loop gain of unity will result in infinite gain and an amplifier is unstable. This will make any disturbance to amplify and result in an o/p.

for an amplifier with +ve f/b for any signal present o/p, can build it to oscillations if loop gain is greater than 1.

→ Conditions for oscillations (Barkhausen criteria).

Oscillators are the device that generate continuous waveform without any ac i/p but given the dc supply etc.

→ The feedback must be positive (phase shift -360°)

→ over all loop gain should be greater than / equal to 1 ($|AvB| \geq 1$). for sustained oscillations

→ Design of oscillator :-

→ To create an oscillator we need amplifier with sufficient gain.

→ f/b n/w that provides phase of 180°.

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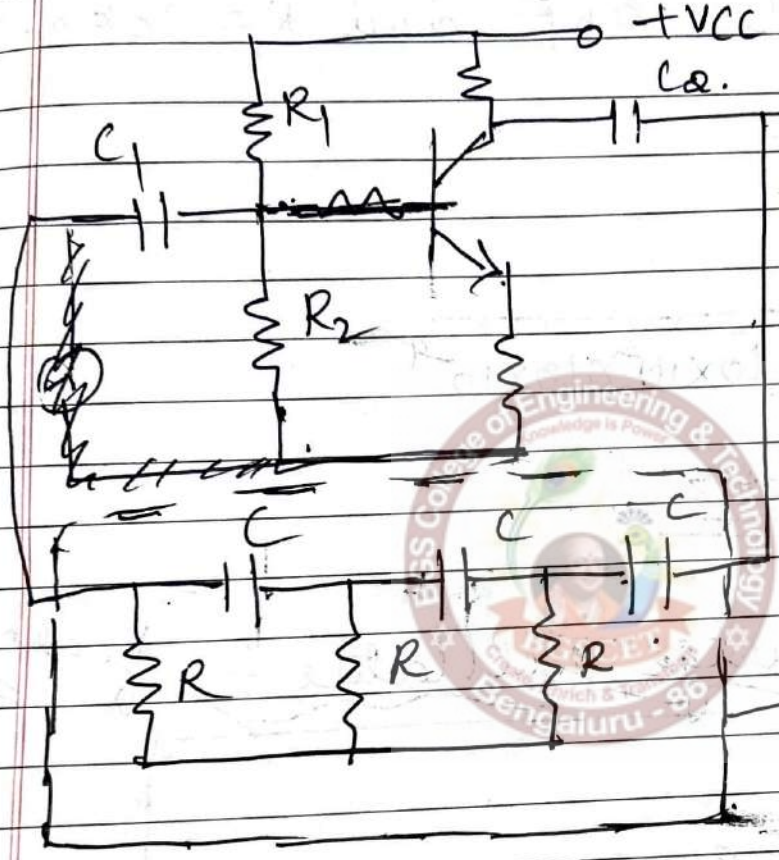
Types of oscillator :-

RC ladder oscillator.



The o/p of amplifier with 180° phase shift is fed to RC n/w. The fb n/w has 3 sections of RC n/w. Each R-C section provides phase shift of ~~180°~~ 60°. So total phase shift of fb n/w is ~~180°~~.

freq of oscillation $f = \frac{1}{2\pi\sqrt{6}RC}$.

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for circuit to oscillate amplifier should provide a gain of 29.

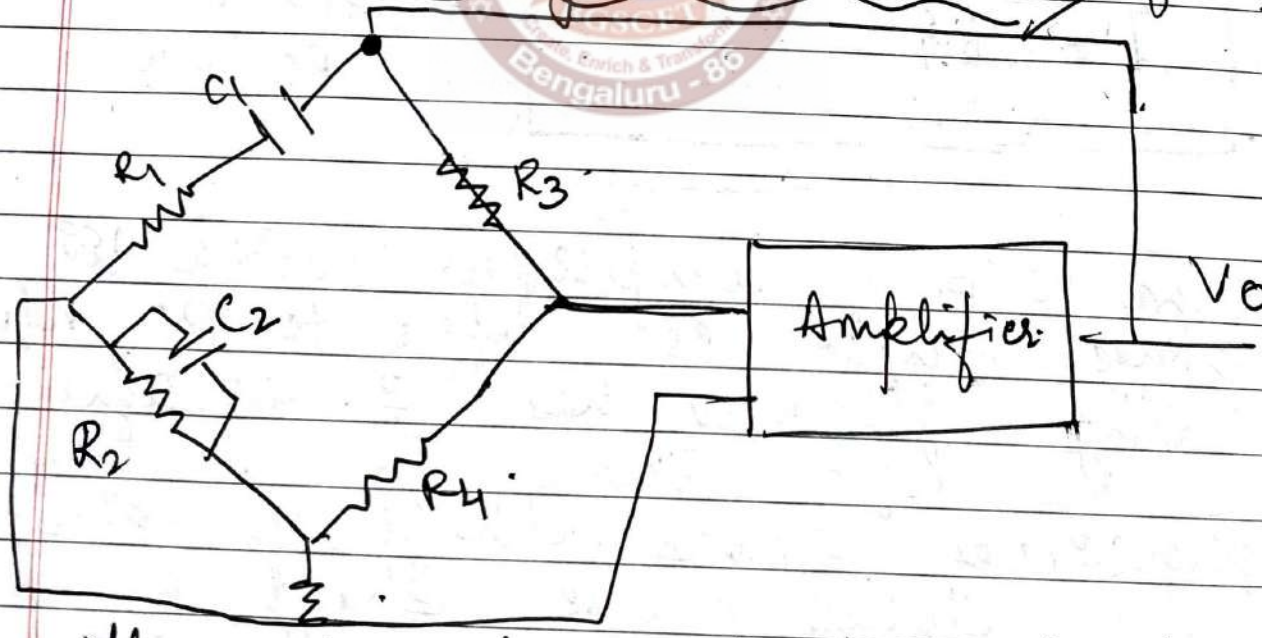
→ Determine the freq of oscillation of a ladder n/w oscillator where C = 10nF and R = 10kΩ.

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

$$f = \frac{1}{2\pi\sqrt{6}\times 10\times 10^{3}\times 10\times 10^{-9}}$$

$$f = 647\,Hz$$

→ Wein Bridge oscillator :- feedback



The o/p of amplifier is fed back to the I/p n/w.

freq of oscillation

$$f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \quad R_1 = R_2 = R,\ C_1 = C_2 = C$$

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Min amp gain required for Sustain Oscillation

$$A_V = 1 + \frac{C_1}{C_2} + \frac{R_2}{R_1}.$$

min amp gain must be 3.

→ The Wein Bridge oscillator having $C_1 = C_2 = 100nF$. find the freq of oscillation if

① $R_1 = R_2 = 1k\Omega$

② $R_1 = R_2 = 6k\Omega$.

$$f = \frac{1}{2\pi\sqrt{RC}}$$

$R_1 = R_2 = R$, $C_1 = C_2 = C$.

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} = \frac{1}{2\pi RC}.$$

$$f = \frac{1}{2\pi \times 1k \times 100 \times 10^{-9}}$$

$$f = 1.592\ KHz.$$

if $R_1 = R_2 = 6k$. $f = \frac{1}{2\pi \times 6k \times 100 \times 10^{-9}}$

$$f = 265.4\ Hz$$

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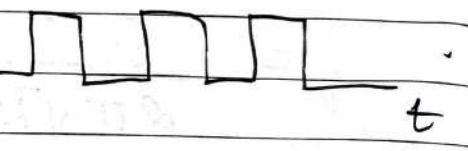
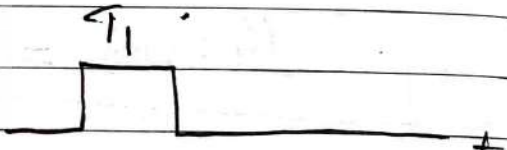
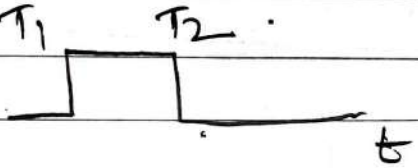
→ **Multivibrators :-**

Multivibrators are a family of oscillator circuits that produce output waveforms consisting of one or more rectangular pulses.

Multivibrators use +ve feedback. Active devices present within the oscillator circuit are operated as switches.

Types of Multivibrator :-

Input	Circuit	output
None	Astable multivibrator	
T	Monostable Multivibrator	
T_1, T_2	Bistable multivibrator	

→ **Astable multivibrators :-**

Provide a continuous train of pulses. (called as free-running oscillators)

→ **Monostable Multivibrators :-** produces

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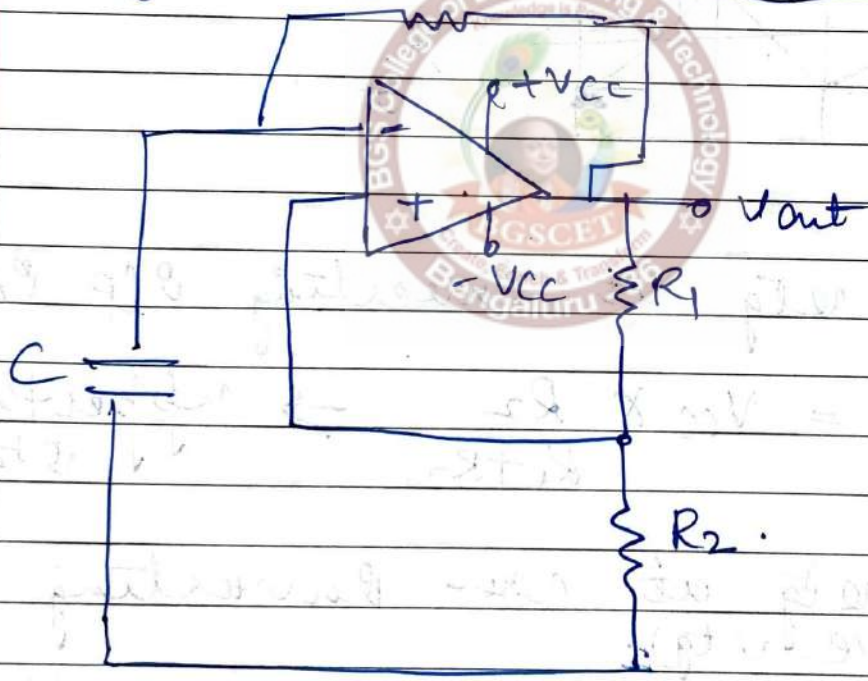
Single o/p pulse - they have one stable state and thus called one-shot.

→ Bistable Multivibrators :- Have two stable states. Require trigger pulse or control signal to change from one state T_1 to another T_1.

→ Single Stage Astable Oscillator :-



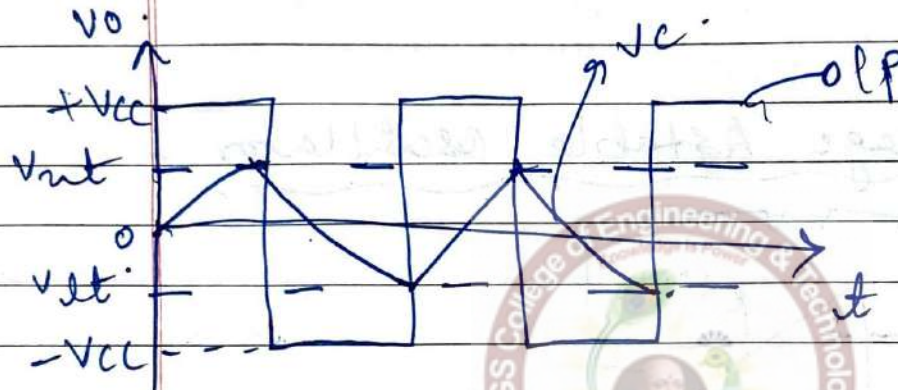
Single stage astable oscillator produces square wave as o/p

+ve fb is given via potential divider formed by R_1 and R_2.

C is initially not charged. Vfg at inverting terminal is

less than vtg at non-inverting terminal.

Hence o/p will rise to $+V_{cc}$. Capacitor C gets charged through R_1. Now vtg at inverting terminal becomes greater than non inverting terminal and o/p is $-V_{cc}$. Hence o/p swings between $+V_{cc}$ and $-V_{cc}$.



Max vtg at inverting o/p is

$$V_{ut} = V_{cc} \times \frac{R_2}{R_1 + R_2} \rightarrow \text{upper threshold vtg}$$

Max vtg at non-inverting o/p. (-ve vtg).

$$V_{lt} = -V_{cc} \frac{R_2}{R_1 + R_2} \rightarrow \text{lower threshold vtg}$$

- when o/p V_{cc} reaches upper threshold vtg capacitor charges.
- when o/p $-V_{cc}$

During +Vcc capacitor starts charging. It charges till V upper threshold point.

One Vut is reached it starts discharging till Vlt lower threshold vtg point is reached.

This charging and discharging continues.

Thus A-stable multivibrator generates square wave without any I/P.

The time for one complete cycle of O/P waveform produced by astable oscillator is

$$T = 2CR\left[1 + 2\left(\frac{R_2}{R_1}\right)\right].$$

→ Crystal Controlled Oscillator:-

To obtain a very high level of oscillator, a Quartz crystal is used as freq determining device. It produces high freq stability in oscillators.

Such oscillators are called Crystal oscillators.

The Quartz crystal - thin slice of Quartz scaled vibrates whenever a potential difference is applied across it. This is known as piezoelectric effect.

The freq of oscillation is determined by Crystal.

The fundamental freq is 100kHz to around 20 MHz.

The freq sensitivity arms of Wein Bridge oscillator uses $C_1 = C_2 = 0.01\mu F$ and $R_1 = 10k\Omega$. freq is varied from 10k to 50kHz find max and min value of R_2

$$f = \frac{1}{2\pi\sqrt{RC}}$$

$$10 \times 10^3 = \frac{1}{2\pi\sqrt{10k \times R2 \times 0.01\mu \times 0.01\mu}}$$

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$f =$

$$f = \frac{1}{2\pi\sqrt{RC}}$$

$$50 \times 10^3 = \frac{1}{2\pi\sqrt{10k \times R_2 \times 0.01\mu \times 0.01\mu}}$$

$R_2 =$ ~~6.5k~~

$R_2 = 10.14\ \Omega$

→ Operational Amplifiers:

→ An amplifier with a gain of 8 has 10% of its o/p fed back to the i/p. Determine the gain.
with -ve flb.
with +ve flb.

$A_v = 8 \quad \beta = 0.1.$

$$A_f = \frac{A_v}{1 + A_v\beta} = \frac{8}{1 + 0.8}$$

$$= 4.44$$

$$A_f = \frac{A_v}{1 - A_v\beta} = \frac{8}{1 - 0.8} = 40$$

→ A phase shift oscillator is to operate with an o/p at 1kHz. If oscillator based on 3-stage ladder n/w determine reqd value of resister if 3-capacitors of 10nF are to be used.

$$f = \frac{1}{2\pi\sqrt{6}RC}.$$

$$1 \times 10^3 = \frac{1}{2\pi\sqrt{6} \times R \times 10 \times 10^{-9}}$$

$$R = 6.5 k\Omega$$

→ A Wein Bridge oscillator based on has R_1 and R_2. If $C_1 = C_2 = 22nF$. Determine values of R_1 and R_2 to produce an o/p of 400Hz.

$$f = \frac{1}{2\pi RC}$$

$$400 = \frac{1}{2\pi \times R \times 22 \times 10^{-9}}$$

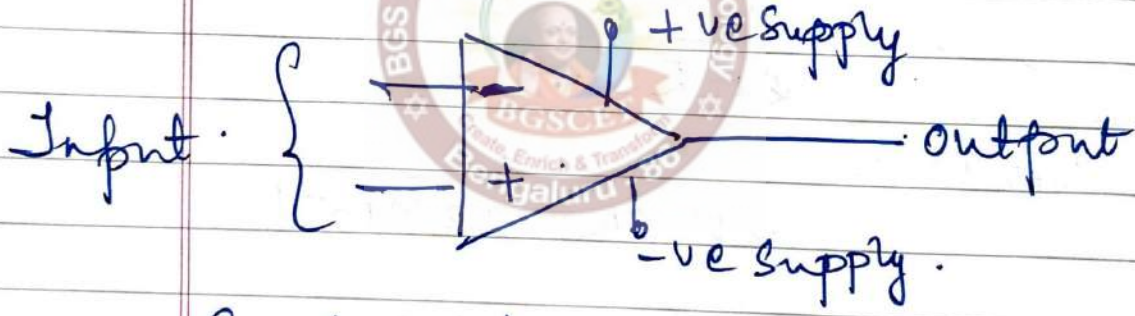
$$R = 16.09 k\Omega$$

Operational Amplifier: Op amp

Opamp is an integrated circuit (IC) fundamental building block for many electronic circuits.

It is high gain negative feedback amplifier used to amplify both ac and dc signals. It is an active element.

Symbol for opamp:-

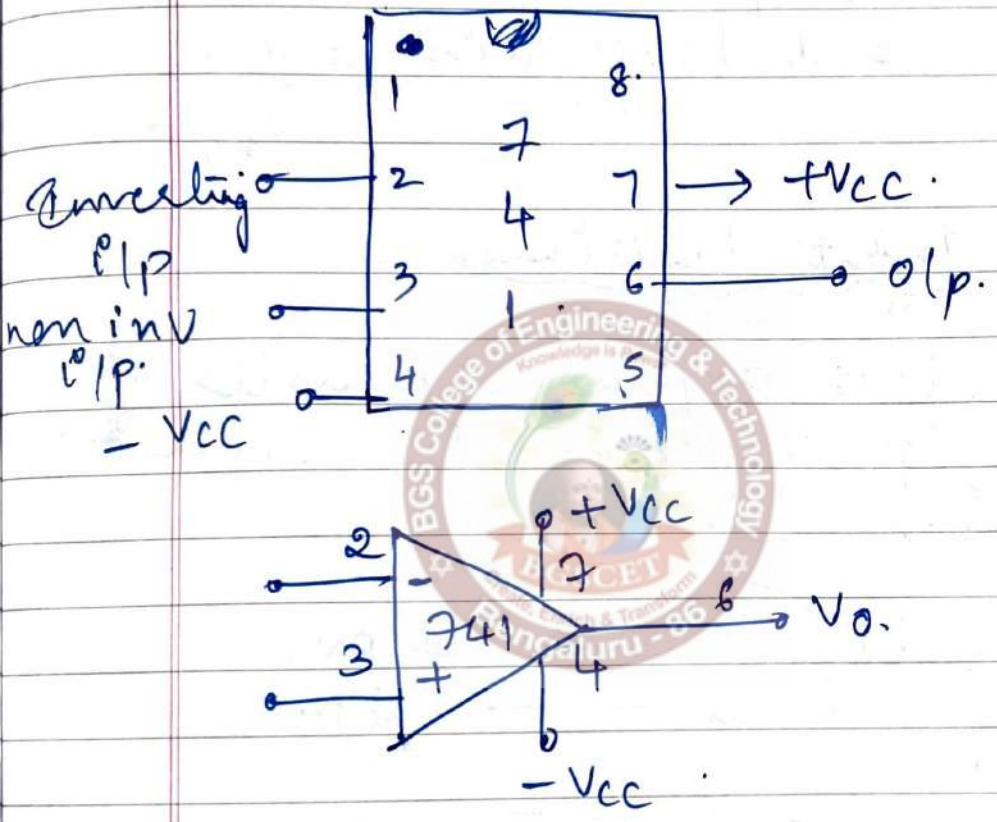


Symbol for an opamp is as shown.

It has two inputs.
'-' inverting i/p.
'+' non-inverting i/p.
It has +ve supply and -ve supply.
'-' indicates 180° phase shift
'+' indicates zero phase shift.

The power supply is from ±5V to ±15V.

Pin Diagram of MA 741.



Op amp parameters :-

→ Open Loop voltage Gain :- (Aol)

Gain of the device without any feedback.

Open loop vtg gain = $20 \log \frac{V_o}{V_{in}}$

Ideal value = ∞ practical value 2×10^5

→ Closed loop vtg Gain :- (A_{cl})

The gain as ratio of o/p to o/p vtg with small proportion of o/p fed back to i/p

Closed loop gain = $\frac{V_{out}}{V_{in}}$.

→ Input Resistance :-

It is defined as ratio of i/p vtg to i/p current.

$R_{in} = \frac{V_{in}}{I_{in}} \cdot \Omega$

Ideal value = ∞.

Practical -u — 2MΩ.

→ output Resistance :-

It is defined as ratio of o/p vtg to o/p current

$R_o = \frac{V_o}{I_o}$ Ω.

Ideal value = 0.

Practical -u — 10Ω to 100Ω.

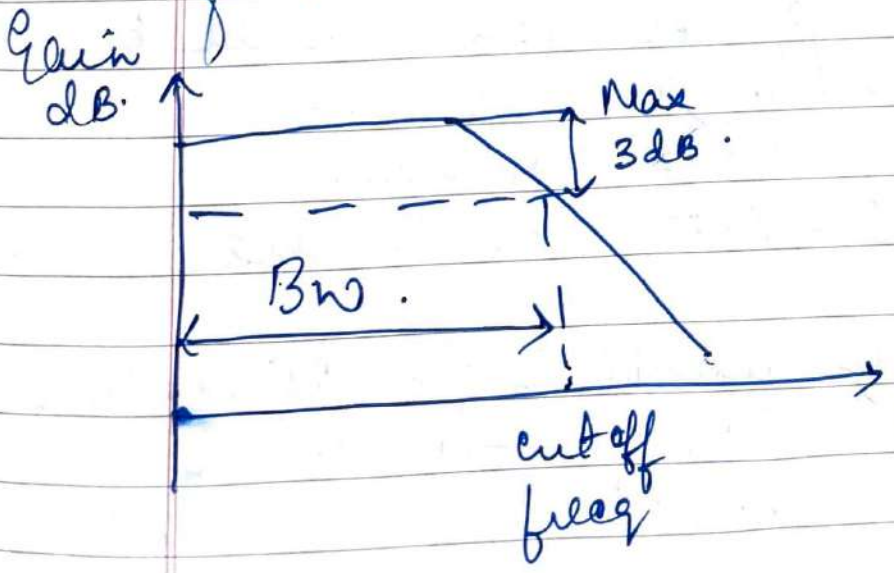
→ I/p offset voltage:

An ideal opamp would provide zero o/p vtg when 0v is applied to its i/p. But in opamp some o/p vtg appears very small even if i/p is zero. The vtg that must be applied to opamp to make this o/p vtg zero is called I/p offset vtg.

Ideal opamp = 0.
practical = 1mV - 15mV.

→ Full power Band Width:

It is range of freq's at which upper max gain falls to 0.707 value.



→ Slew Rate:

Slew rate of an opamp is rate of change of o/p w.r.t with time when the o/p is given.

$$SR = \frac{dV_o}{dt} \quad V/\mu s.$$

measured in V/μs.

Typical value range from 0.2V/μs — 20V/μs

→ Parameters of opamp or characteristics:

→ open loop gain should be high

→ i/p resistance should be high

→ o/p resistance should be low.

→ Full power BW should be as wide as possible

→ Slew rate large.

→ I/p offset should be small.

Note: If o/p applied to inverting terminal and non-inverting grounded then it is inverting opamp

Ideal and Practical values for opamp.

Parameter	Ideal	Practical.
Voltage gain	Infinite	100,000.
I/p resistance	Infinite	100MΩ.
o/p resistance	Zero.	20Ω.
BW.	Infinite	2MHz.
Slew rate	Infinite	10V/μs.
I/p offset.	Zero	less than 5mV.

→ An opamp operating with -ve f/b produces an o/p voltage of 2V when supplied with an I/p of 400μV. Determine closed loop V/g gain.

$$A_{cl} = \frac{V_{out}}{V_{in}} = \frac{2}{400 \times 10^{-6}}$$

$$= 5000.$$

Gain in dB = $20 \log(5000)$

$$= 74 \text{ dB}.$$

Module - 3.

Boolean Algebra and Logic Circuits

→ Number System Representation:

Decimal System:

Decimal number system is very simple and easy to perform any mathematical operations.

The numbers in Decimal System are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9. So there are 10 numbers. It is called Base 10. Representation is $(1240)_{10}$.

$(A_n, A_{n-1}, A_{n-2} \ldots A_0, A_{-1}, A_{-2} \ldots A_{-n})_r$

Base or radix (r)

$$A_n r^n + A_{n-1} r^{n-1} + A_{n-2} r^{n-2} \ldots A_0 r^0 + A_{-1} r^{-1} + A_{-2} r^{-2} \ldots A_{-n} r^{-n}$$

A_n is most significant digit

A_{-n} is least significant digit

A3 A2 A1 A0

$(1240)_{10} = 1\times10^3 + 2\times10^2 + 4\times10^1 + 0\times10^0$

$= 1000 + 200 + 40 + 0$

$= 1240$

→ Binary System:

Binary system has only two state zero or One '0' or '1'.

Hence it is called Base two system or radix is 2.

Ex $(1101)_2$ → Binary Num.

→ Binary to Decimal Conversion:

→ Convert $(1001.110)_2$ to decimal System.

Sol^n: $(1001.110)_2$

$b_4\ b_3\ b_2\ b_1\ b_0 . b_{-1}\ b_{-2}\ b_{-3}$

$1\times2^4 + 1\times2^3 + 0\times2^2 + 0\times2^1 + 1\times2^0 +$

$1\times2^{-1} + 1\times2^{-2} + 0\times2^{-3}$

$16 + 8 + 1 + 0.5 + 0.25$

$= (25.75)_{10}$

→ Convert $(1110.111)_2$ to decimal system.

Sol:-

$$1\times2^3 + 1\times2^2 + 1\times2^1 + 0\times2^0 + 1\times2^{-1} + 1\times2^{-2} + 1\times2^{-3}$$

$$= 8 + 4 + 2 + 0 + 0.5 + 0.25 + 0.125$$

$$= (14.875)_{10}$$

Extra problems:

Convert the following Binary to Decimal

Q) i):

→ $(101010)_2$

→ $(0.110)_2$

→ $(101011 0.1101)_2$.

→ Decimal to Binary Conversion:

→ Convert $(105.202)_{10}$ to Binary system.

2	105	
2	52	- 1
2	26	- 0
2	13	- 0
2	6	- 1
2	3	- 0
	1	- 1

1 1 0 1 0 0 1.

$.202 \times 2 = 0.404$, $C = 0$.

$0.404 \times 2 = 0.808$, $C = 0$.

$0.808 \times 2 = 1.616$, $C = 1$

$0.616 \times 2 = 1.232$, $C = 1$.

$= (0011)_2$

So $(1101001.0011)_2$

→ Convert $(1024.625)_{10}$ to binary system.

2	1024	
2	512	→ 0
2	256	→ 0
2	128	→ 0
2	64	→ 0
2	32	→ 0
2	16	→ 0
2	8	→ 0
2	4	→ 0
2	2	→ 0
	1	→ 0

$(10000000000)_2$

0.625 x 2 = 1.250, C = 1

0.250 x 2 = 0.50, C = 0.

0.5 x 2 = 1.0, C = 1.

$(.101)_2$

$(10000000000.101)_2$

Extra problems:

Convert the following decimal to Binary number s/m.

→ $(555)_{10}$ → $(65.45)_{10}$

→ $(0.825)_{10}$.

→ Octal number System:

Octal number system have 8 possible levels or symbols from 0, 1, 2, 3, 4, 5, 6, 7. It has eight numbers from 0-7. So, Base 8 or Octal System.

→ Octal to Decimal conversion

→ Convert $(2026)_8$ to decimal

$2 \times 8^3 + 0 \times 8^2 + 2 \times 8^1 + 6 \times 8^1$

$= (1046)_{10}$

→ Convert $(204.2)_8$ to decimal

$2 \times 8^2 + 0 \times 8^1 + 4 \times 8^0 + 2 \times 8^{-1}$

$= 128 + 4 + 0.25$

$= (132.25)_{10}$

→ Extra problems:

→ Convert the following Octal numbers to Decimal numbers.

→ $(1234.56)_8$

→ $(0.625)_8$

→ $(1722)_8$.

→ Decimal to Octal Conversion:

→ Convert $(576)_{10}$ to Octal.

8 | 576
8 | 72 — 0
8 | 9 — 0
1 — 1

→ $(1100)_8$.

→ Convert $(985.85)_{10}$ to Octal.

8 | 985
8 | 123 — 1
8 | 15 — 3
1 — 7

$(1731)_8$

$0.85 \times 8 = 6.80 \rightarrow C = 6$

$0.80 \times 8 = 6.40 \rightarrow C = 6$

$0.40 \times 8 = 3.20 \rightarrow C = 3$

$0.20 \times 8 = 1.60 \rightarrow C = 1$

$0.60 \times 8 = 4.80 \rightarrow C = 4$

$(.6631)_8$

$\Rightarrow (1731.66314)_8$

→ Extra problems:

Convert the following Decimal to Octal s/m:

→ $(284.65)_{10}$.

→ $(532.65)_{10}$.

→ Hexadecimal number System:

This number system is used on microprocessor, micro-controllers and computers.

It has 16 numbers from 0 to 9 and 10 to 15.

10 to 15 represented by A to F.

This is base 16 or radix 16 number s/m.

Decimal number — 0 to 9.
Octal — 0 to 7.
Binary — 0 & 1.
Hexa — 0 to 9 and A to F.

Decimal Number	Binary Num	Hexa decimal.
0	0000	0.
1	0001	1
2	0010	2.
3	0011	3
4	0100	4
5	0101	5.
6	0110	6.
7	0111	7.
8	1000.	8.
9	1001	9.
10	1010.	A.
11	1011	B.
12	1100	C.
13	1101	D.
14	1110	E.
15	1111	F.

Convert $(5)_{10}$ to Binary.

2 | 5
2 | 2 - 1
1 - 0

$(101)_2$

→ Convert $(13)_{10}$ to binary:

2 | 13
2 | 6 - 1
2 | 3 - 0
1 - 1

$(1101)_2$

→ Decimal to HexaDecimal Conversion:

→ Convert $(988.86)_{10}$ to hexadecimal number s/m.

16 | 988
16 | 61 - 12 (C)
3 - 13 (D)

0.86 x 16 = 13.76 C = 13 - (D)
.76 x 16 = 12.16 C = 12 (C) ↓
.16 x 16 = 2.56 C = 2
.56 x 16 = 8.96 C = 8

$(3DC.DC28)_{16}$

→ Convert $(124)_{10}$ to hexadecimal

16 | 124
7 - 12 (C) ↑ $= (7C)_{16}$.

→ Extra problems:

→ Convert the following decimal to hexa decimal num s/m.

→ $(526.44)_{10}$

→ $(483.50)_{10}$.

→ Hexadecimal to Decimal Conversion

→ Convert $(ABC.CD)_{16}$ to decimal number s/m.

2 1 0 -1 -2.

A B C . C D
(10) (11) (12) (12) (13)

$10 \times 16^2 + 11 \times 16^1 + 12 \times 16^0 + 12 \times 16^{-1} + 13 \times 16^{-2}$.

$= (2748.80)_{16}$

→ Convert $(9CF1)_{16}$ to decimal num s/m.

$9\ C\ F\ 1$
$3\ 2\ 1\ 0$

$9 \times 16^3 + 12 \times 16^2 + 15 \times 16^1 + 1 \times 16^0$

$= (40177)_{10}$.

→ Extra problems

→ Convert $(1A6.C8)_{16}$ to decimal num s/m.

→ Convert $(214.A66)_{16}$ to decimal num s/m.

→ Convert $(ABCD)_{16}$ to decimal num s/m.

→ Binary to Octal number s/m:

procedure;

→ Group the given binary digits or bits from RHS to LHS to group of 3. If the last group is

not equal to 3 bits, prefix read num of 0's.

→ Write the corresponding octal number for each groups of binary bits.

→ Go for the binary bits after the decimal carry out above steps from LHS to RHS...

→ Convert $(1110111010.101)_2$ to Octal num s/m.

→ 0 1 1 | 1 0 1 | 1 1 0 | 1 0 1 ←

$(3565)_8$

→ Convert $(.101011)_2$ to Octal num s/m:

→ 0 . 1 0 1 | 0 1 1 .

$(0.53)_8$

→ Convert $(010110101001.101011000)_2$ to Octal s/m.

$010|110|101|001$

2 6 5 1

$101|011|000$

5 3 0

$= (2651.530)_8$

→ Octal to Binary System.

→ for the given Octal num write each digit as bits of three in binary.

→ Convert $(3565)_8$ to binary s/m.

3 5 6 5

$(011|101|110|101)_2$

→ Convert $(2651.53)_8$ to Binary s/m.

2 6 5 1 . 5 3 .

$(010\ 110\ 101\ 001.\ 101\ 011)_2$

→ Binary To Hexadecimal Conversion :

→ Convert $(101101010001.101011)_2$ to hexadecimal s/m.

0.1 0 1 1 0 1 0 1 0 0 0 1 . 1 0 1 0 1 1 0 0

5 A 9 . A C .

$(5A9.AC)_{16}$

→ Convert $(0.10000100)_2$ to hexadecimal s/m.

0 . 1 0 0 0 0 1 0 0 .

$(0.84)_{16}$

→ Extra problems:-

→ Convert $(1010.011)_2$ to decimal

Sln:

$1\times2^3 + 0\times2^2 + 1\times2^1 + 0\times2^0 + 0\times2^{-1} + 1\times2^{-2} + 1\times2^{-3}$.

$= (10.375)_{10}$

→ Convert $(630.4)_8$ to decimal

Sln:

$6\times8^2 + 3\times8^1 + 0\times8^0 + 4\times8^{-1}$

$= (408.5)_{10}$

→ Convert $(41)_{10}$ to Binary:

2 | 41
2 | 20 - 1
2 | 10 - 0
2 | 5 - 0
2 | 2 - 1
1 - 0

$(101001)_2$

→ Convert $(153)_{10}$ to Octal

8 | 153
8 | 19 - 1
2 - 3

$(231)_8$.

→ Convert $(0.6875)_{10}$ to Binary

Ex $0.6875 \times 2 = 1.3750$, C=1
$0.3750 \times 2 = 0.750$, C=0 ↓
$0.750 \times 2 = 1.50$, C=1
$0.50 \times 2 = 1.00$ C=1

$(0.1011)_2$

→ Convert $(0.513)_{10}$ to Octal

$0.513 \times 8 = 4.104$ → C=4 ↓
$0.104 \times 8 = 0.832$ → C=0
$0.832 \times 8 = 6.656$ → C=6
$0.656 \times 8 = 5.248$ C → 5
$0.248 \times 8 = 1.984$ C=1

$(0.40651)_8$

→ Convert $(.1\,1\,0\,0\,0\,1\,\ 1\,0\,1\,\ 0\,1\,1\,.\,1\,1\,1\,\ 1\,0\,0\,\ 0\,0\,0\,\ 1\,1\,0)_2$ to Octal

$\therefore$ | 0 | 1 1 0 | 0 0 1 | 1 0 1 | 0 1 1 . 1 1 1 | 1 0 0 | 0 0 0 | 1 1 0 .

$(26153.7406)_8$

→ Convert $(10110\,0110\,1011.1111\,0010)_2$ to hexadecimal s/m.

$10 \mid 1100 \mid 0110 \mid 1011.1111 \mid 0010$

$(2\ C\ 6\ B\ .\ F\ 2)_{16}$

→ Convert $(673.124)_8$ to Binary num s/m.

$6\ 7\ 3\ .\ 1\ 2\ 4$

$(110\,111\,011.001\,010\,100)_2$

→ Convert $(306.D)_{16}$ to Binary num.

$3\ 0\ 6\ .\ D$

$(0011\,0000\,0110.1101)_2$

→ Complements:-

Complements are used in digital computers for simplifying subtraction

operations.

There are two types of complements for each r system and r-1 system.

If base / radix is 2 in binary system there are 2's complement and 1's complement.

If base / radix is 9 then in decimal system there are 9's complement and 10's complement.

(r-1) complement is called diminished radix complement

→ 1's Complement Representation

The 1's complement of binary number is obtained by replacing all 1's by 0's and all 0's by 1's.

→ Find 1's Complement of $(11011)_2$

⇒ 1 1 0 1 1

1's Comp = $(00100)_2$

→ Find 1's Complement of $(1011100011)_2$

⇒ $(0100011100)_2$

→ 2's Complement :-

2's complement is obtained by first taking 1's complement and add '1' to the result (LSB).

→ Find 2's complement of $(110011)_2$

⇒ 00 11 00

+ 1

$(00\ 1\ 1\ 0\ 1)_2$ ← 2's complement

→ Find 2's complement of $(1010000011)_2$

⇒ 0 1 0 1 1 1 1 0 0

+ 1

$(0\ 1\ 0\ 1\ 1\ 1\ 1\ 0\ 1)_2$

→ 9's Complement Representation

9's complement is obtained by subtracting each digit of given number from digit 9.

→ Find 9's complement of $(865)_{10}$.

→ 9 9 9
− 8 6 5
(1 3 4)

→ Find the 9's complement of $(10875)_{10}$.

→ 9 9 9 9 9
− 1 0 8 7 5
8 9 1 2 4

→ 10's Complement Representation

10's complement is obtained by first taking 9's complement and adding '1' to the result.

→ Find 1's Complement of $(879)_{10}$.

→
$$\begin{array}{r} 999 \\ -\ 879 \\ \hline 120 \\ +\ \quad 1 \\ \hline 121 \end{array}$$

→ Find 1's complement of $(10213)_{10}$.

$$\begin{array}{r} 99999 \\ -\ 10213 \\ \hline 89786 \\ +\ \quad 1 \\ \hline (89787) \end{array}$$

→ Binary Addition

0 + 0 = 0, C = 0
0 + 1 = 1, C = 0
1 + 0 = 1, C = 0
1 + 1 = $(10)_2$
1 + 1 + 1 = $(11)_2$

1 + 1 = 2
In Binary
2 = (10)

→ 1's Complement Subtraction :-

Steps :-

→ Take 1's complement of the subtrahend.
→ Add it to Minuend
→ If carry is generated add carry to the LSB of the result. If no carry then take 1's complement of ans & '-' sign
→ $(10111)_2 - (11010)_2$ using 1's Complement.

⇒ M → 10111
S → 11010.

1's Complement → 00101.

```
  1 1 1
  10111
+ 00101
-------
  11100
-------
```

1's Complement of ans → 00011

$= -(00011)_2$

⇒ Subtract $(11010)_2 - (10111)_2$ using 1's Complement method.

⇒ S → 11010 → 1's cmp → 01000.
M → 10111

```
  1 1 0 1 0
+ 0 1 0 0 0
-----------
  0 0 0 1 0
```

Carry → 1

$(00011)_2$

→ Subtract $(10101010)_2$ from $(11100010)_2$

⇒ S → 11100010 → 1's
M → 10101010

```
  0 1 0 1 0 1 0 1
  1 1 1 0 0 0 1 0
+ 0 1 0 1 0 1 0 1
-----------------
  0 0 1 1 0 1 1 1
+ 1 1 1 1 1 1 1 1
-----------------
  0 0 1 1 1 0 0 0
```

$(00111000)_2$

→ Subtract $(1110000)_2$ from $(1010100)_2$ using 2's Complement.

⇒ S → 1010100.
M → 1110000 1's comp.

0001111

1 0 1 0 1 0 0
+ 0 0 0 1 1 1 1
1 1 0 0 0 1 1 1

No carry take 1's complement & place -ve sign
$-(0011000)_2$

→ 2's Complement Subtraction:

→ take 2's complement of minuend
→ Add it to Subtrahend.
⇒ If Carry is generated ~~add it to LSB of result~~ discard it
→ If no carry take 2's complement of result and place -ve sign.

→ Subtract $(1010111)_2$ from $(1110011)_2$ using 2's complement.

→ S → 1110011
M → 1010111 — 2's comp

```
  0101000
+        1
---------
  0101001
```

```
  1110011
+ 0101001
---------
(1)0011100
```

Carry (neglect) ans = $(0111\,00)_2$

→ Subtract $(11010)_2$ from $(11101)_2$ using 2's complement.

S → 11101
or → 11010 — 2's

```
  00101
+     1
---------
  00110
```

```
  11101
+ 00110
---------
(1)00011
```

Ignore carry.

$(00011)_2$

→ Subtract $(111001)_2$ from $(101011)_2$ using 2's complement.

⇒ S → 101011
M → 111001 — 2's comp:

```
  000110
+       1
  ------
  000111
```

```
  101011
+ 000111
  ------
  110010
```

no carry take 2's complement & place '-' sign

```
  001101
+       1
  ------
-(001110)2
```

→ Subtract $(11101)_2$ from $(11010)_2$ using 2's complement.

⇒ S → 11010
M → 11101 — 2's Comp

```
  00010
+     1
-------
  00011
```

```
  11010
+ 00011
-------
  11101
```

no carry take 2's Complement & place − sign

```
  00010
+     1
-------
 (00011)2
-------
```

→ Subtract 1.0101100 − 1000011 using 1's complement.

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Page

S = 1010100 , M = 1000011 → 1's comp. 0111100.

```
    1010100
  + 0111100
  (1) 0010000
  C└──────→    1
  ─────────────
  (0010001)₂
```

→ Subtract $(1000011)_2 - (1010100)_2$

$\bar{M}$ → 0101011

```
    1000011
  + 0101011
  ─────────
    1101110
```

no carry so take 1's complement

$(-0010001)_2$

extra problems

→ Subtract 1010100 − 1000011 using 2's complement.

→ Subtract 1000011 − 1010100 using 2's Complement.

→ 9's Complement Subtraction

→ Take 9's complement of minuend.
→ Add it to subtrahend.
→ If carry is generated, add it to final result.
→ If no carry take 9's complement.

→ Subtract (176)$_{10}$ from (200)$_{10}$ using 9's complement

$$\begin{array}{r} 999 \\ -\ 176 \\ \hline 823 \end{array}$$

$$\begin{array}{r} 200 \\ +\ 823 \\ \hline 1023 \\ \hline (024)_{10} \end{array}$$

1 → 1

→ Subtract (157)$_{10}$ from (176)$_{10}$ using 9's complement.

$$\begin{array}{r} 999 \\ -\ 157 \\ \hline 842 \end{array}$$

$$\begin{array}{r} 176 \\ +\ 842 \\ \hline 1018 \\ \hline (019)_{10} \end{array}$$

1 + 7 → 1

→ Subtract $(176)_{10} - (200)_{10}$ using 9's complement.

```
  999        176
- 200        799
-----      -----
  799        975
```

no carry.

```
  999
- 975
-----
 (024)
```

$\Rightarrow -(024)_{10}$

→ 10's Complement Subtraction

→ Take 10's complement of minuend
→ Add it to subtrahend.
→ If carry is generated discard it.
→ If no carry take 10's complement of ans & place -ve sign.

→ Subtract $(729)_{10}$ from $(122)_{10}$ using 10's complement.

```
  999
- 729
-----
  270
+   1
-----
  271
```

```
  122
+ 271
-----
  393
```

no carry take 10's complement

```
  999
- 393
-----
  606
+   1
-----
-(607)10
```

⇒ Using 10's Complement Subtract 3250 − 72532.

```
  99999
- 72532
-------
  27467
+     1
-------
  27468
```

```
  03250
+ 27468
-------
  30718
```

no carry.

```
  99999
- 30718
-------
  69281
+     1
-------
  69282
```

⇒ $-(69282)_{10}$

9999
3280
6740

Boolean Algebra :-

→ Boolean algebra is defined as a set of elements, a set of operators and a number of postulates

→ If S is a set, x and y are certain objects then $x \in S$ denotes x is a member of set S.

→ If y does not belong to set S then it is denoted as $y \notin S$

→ $A = \{1, 2, 3, 4\}$. 0, e elements of Set A are 1, 2, 3 & 4.

→ Binary operator denoted by * defined on Set S of elements is a rule that assigns to each pair of elements from S a unique element from S.

→ $a * b = c$

→ * is binary operator where $a, b, c \in S$.

→ * is not a binary operator if $a, b \in S$ whereas $c \notin S$.

→ Postulates for Boolean Algebraic Structure

→ Closure: A set S is said to be w.r.t a binary operation $a * b = c$. If $a, b \in S$ and also $c \in S$.

→ Associative Law:

A binary operator * is said to be associative if $(x * y) * z = x * (y * z)$ $x, y, z \in S$.

→ Commutative Law:

A binary operator * is said to be Commutative if $(x * y) = (y * x)$, $x, y \in S$.

→ Identity Element:

A set S is said to have an Identity elem

such that

$x * e = x$, $x \in S$.

'0' is identity element for addition.

'1' is identity element for multiplication.

→ Inverse : A set S is said to have inverse element $x * y = e$.

Ex: If a is element inverse of a will be $a - a = 0$ under addition

→ Distributive Law :

$x * (y \cdot z) = (x * y) \cdot (x * z)$

Note: Binary operator '+' defines addition.

Additive Identity is 0.

multiplicative Identity is 1.

additive Inverse defines Subtraction

multiplicative Inverse of a

is ½.

→ Axiomatic Definition of Boolean Algebra:-

→ Boolean algebra is an algebraic structure defined on set of elements B together with two binary operators '+' and '.' provided following Huntington postulates are satisfied.

1. → closure with respect to the operator '+'.
   → closure w.r.t operator '.'

2. → x+0 = x or 0+x = x. identity element for addition is 0.
   → 1.x = x.1 = x, identity element w.r.t multiplication is 1

3. → x+y = y+x } Commutative
   → xy = yx } law

→ . is distributive over '+'
x.(y+z) = xy + xz.

→ 4. { '+' is distributive over '.'
$x + (y \cdot z) = (x + y) \cdot (x + z)$.

5. → For every element $x \in B$.
There exists $x' \in B$.
(called Complement of x)
Such that $x + x' = 1$
$x \cdot x' = 0$

6 → There exists two Complement elements $x, y \in B$ such that $x \neq y$. (Distinct elements)

→ Compare Boolean Algebra with Ordinary Algebra.

	ordinary algebra	Boolean Algebra
→	Deals with real numbers	Deal with 2 elements 0 & 1.
→	Complements not available	Complements are available
→	Distributive law over + & . not available	Distributive law over + & . available.

Conditions to have Boolean Algebra:

→ Elements of set B.
→ Rules of operation for the two Binary operators.
→ Set of elements B together with two Binary operators satisfies Huntington Postulates.

Two Valued Boolean Algebra:

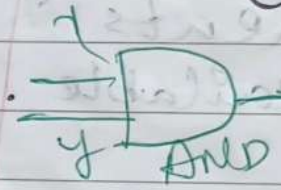
→ A two valued Boolean Algebra is defined on a set of two elements $B = \{0, 1\}$.

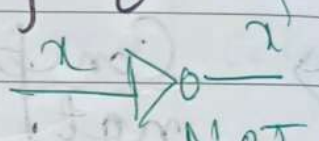
AND

x	y	x.y
0	0	0
0	1	0
1	0	0
1	1	1

NOT

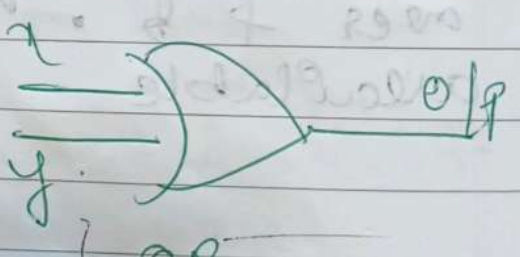
x	x'
0	1
1	0





OR

x	y	x+y
0	0	0
0	1	1
1	0	1
1	1	1



* The rules are And, OR and Not operations.

→ To prove Huntingston postulate for $B = \{0, 1\}$.

→ 1. Closure :- Since result of each operation is either 0 or 1 it belongs to 'B' So closure is satisfied.

→ 2. Identity Element :-

→ $1 + 0 = 1$, $0 + 1 = 1$. for addition.

→ $1 \cdot 1 = 1$, $0 \cdot 1 = 0$ for multiplication.

→ 3. Commutative :- $0 \cdot 1 = 1 \cdot 0 = 0$.

$0 + 1 = 1 + 0 = 1$.

→ 4. Distributive Law :-

$x \cdot (y + z) = xy + xz$.

x	y	z	x.(y+z)	xy	xz	xy+xz
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	0
1	0	1	1	0	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	1

Thus Distributive Law is proved.

→ 5 Complement : $x + x'$ { $0+1=1$, $1+0=1$ } Addition

$x \cdot x' = 0.1 = 0$, $1.0 = 0$ } Multiplication

→ 6 Set B has distinct element 0 & 1 where $1 \neq 0$

Note: This two valued Boolean Algebra is also called Switching Algebra.

→ Basic Theorems and postulates of Boolean Algebra

Duality : Interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

Basic Theorems & Postulates

Postulate 2	$x+0=x$	$x.1=x$
Postulate 5	$x+x'=1$	$x.x'=0$
Theorem 1	$x+x=x$	$x.x=x$
Theorem 2	$x+1=1$	$x.0=0$
Theorem 3. Involution	$(x')'=x$	
Postulate 3 Commutative	$x+y=y+x$	$xy=yx$
Theorem 4 Associative	$x+(y+z)=(x+y)+z$	$x(yz)=(xy)z$
Postulate 4 Distributive	$x(y+z)=xy+xz$	$x+(yz)=(x+y)(x+z)$

→ Theorem-5 Demorgan's	$(x+y)' = x' \cdot y'$	$(xy)' = x' + y'$
→ Theorem-6 Absorption	$x + xy = x$	$x(x+y) = x$

Theorem-1

→ $x + x = x$ [Idempotent property]

$$x + x = (x+x) \cdot 1$$

$$= (x+x)(x+x')$$

$$= x + xx'$$

$$= x$$

$\{ \because (xy)(y+z) = x + yz \}$

∴ proved.

→ $x \cdot x = x$

$$x \cdot x = x \cdot x + 0$$

$$= x \cdot x + x \cdot x'$$

$$= x(x+x')$$

$$= x$$

$\{ xy + xz = x(y+z) \}$

→ Theorem - 2

→ $x + 1 = 1$.

$x + 1 = 1 \cdot (x + 1)$

$= (x + x') (x + 1)$

$= x + x' \cdot 1$

$= x + x'$

$= 1$ ∴ proved.

2)

→ $x \cdot 0 = 0$.

→ Theorem - 3 [Involution]

$(x')' = x$.

↓

$(x)' = x$ ∴ proved.

→ Theorem - 6 [Absorption]

$x + yz = x$

$x + xy$

$x(y+1)$

$x \cdot 1$

$= x$ proved

$\therefore$

$\rightarrow x(x+y)$

$(x+x)(x+y)$

$x + xy$

$x(1+y) = x$ proved.

→ State and prove DeMorgan's theorem :-

Demorgan's theorem states

$(x+y)' = x' \cdot y'$

$(x \cdot y)' = x' + y'$

x	y	(x+y)	(x+y)'	x'	y'	x'y'
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

proved

x	y	xy	(xy)'	x'	y'	x'+y'
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

proved.

→ Note: Representation of Boolean variables is called Boolean expression.

→ Operator Precedence:

The operator precedence to be followed while evaluating Boolean expression

is as follows:

→ Expression inside parentheses
→ Complement
→ AND
→ OR.

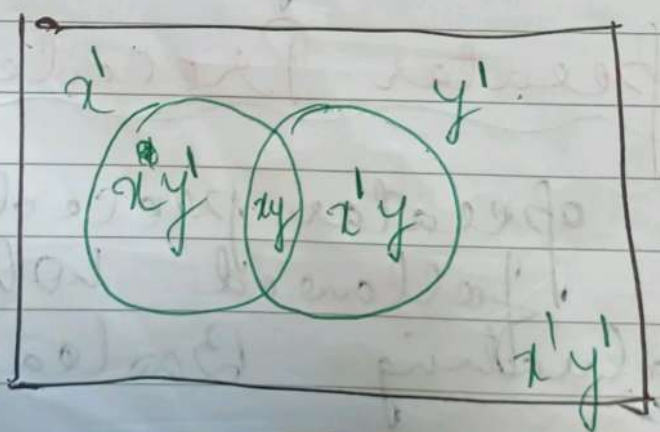
→ Venn Diagram:-

Venn Diagrams used to illustrate the postulates of Boolean Algebra.

It is used to visualize the relationships among variables of Boolean expression.

The diagram consists of a rectangle inside which overlapping circles are drawn. One circle for each variable.

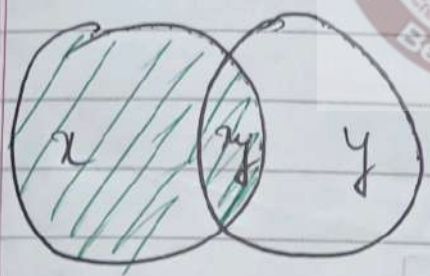
If inside the circle we say $x=1$ if outside we say $x=0$.



We have 2 circles named x & y.
The area within circle x $x=1$ & $y=0$ $x'y$.
The area within circle y, $y=1$ & $x=0$, so xy'
$x'y$. Area of overlapping between x & y is xy.
Area outside x & y is $x'y'$.

→ Venn Diagram To Illustrate $x = xy + x$

(2)

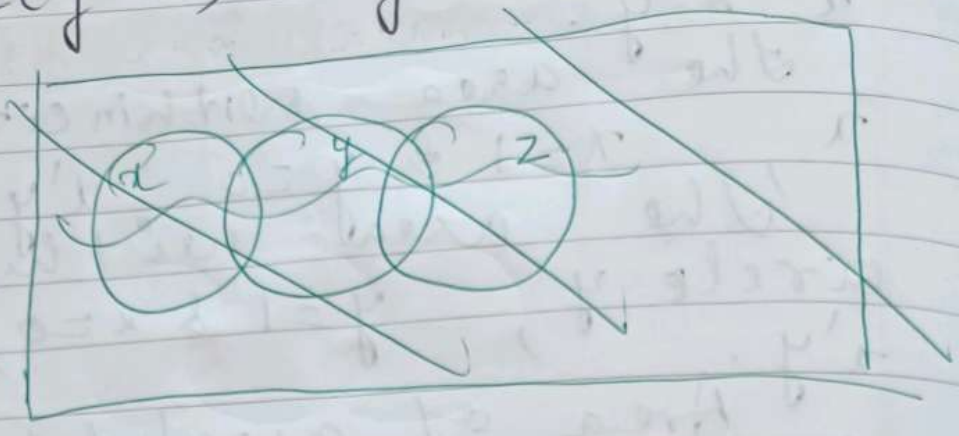


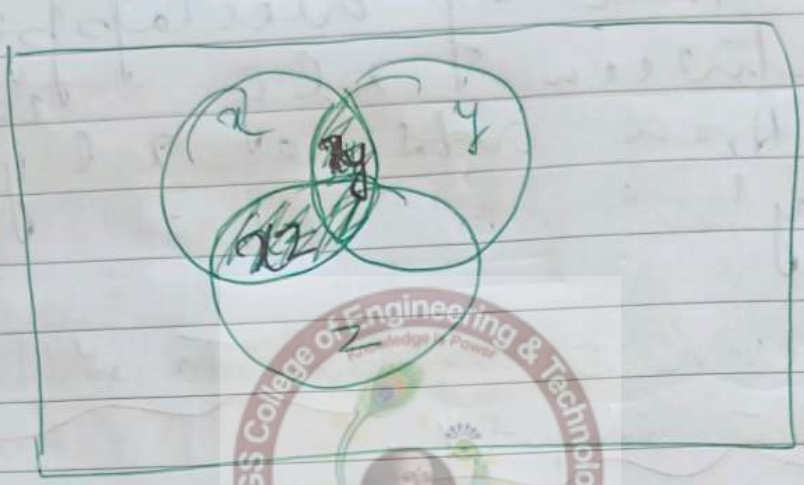
$x = xy + x$

area belonging to xy is inside circle x. So
$x = xy + x$

→ Venn Diagram to Illustrate distributive Law :-

$x(y+z) = xy + xz$.

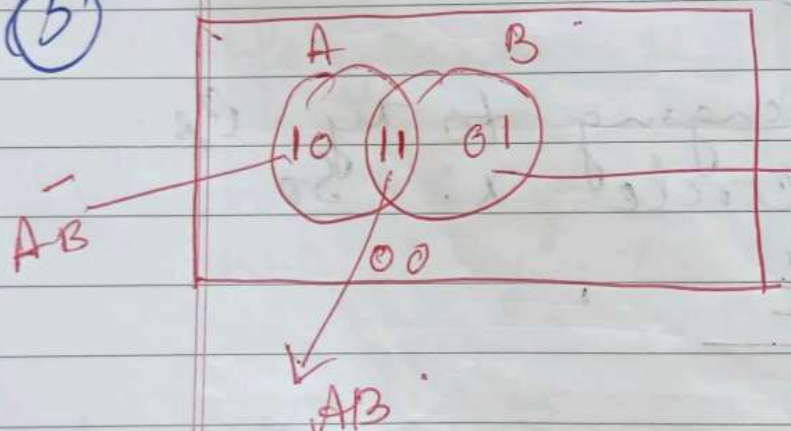




$xy + xz$

→ Examples:-

(3)



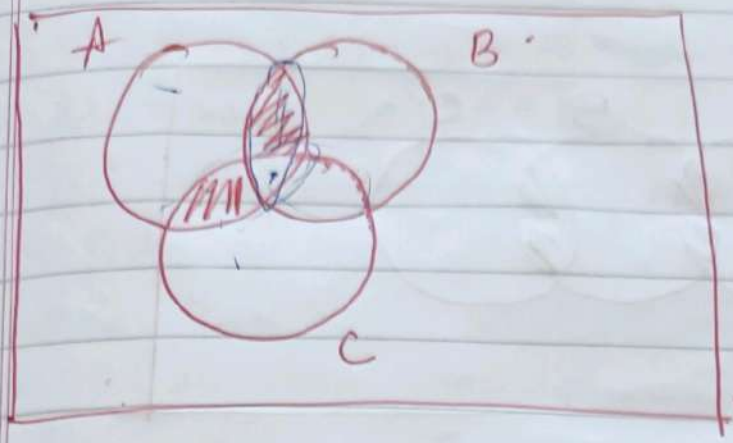
(4)

$X = \bar{A}A\bar{B} + \bar{A}B + A\bar{A}B$.

$X = A(B+\bar{B}) + \bar{A}B$

$X = A + \bar{A}B$.

→ Write the Boolean Expression for Shaded Area:

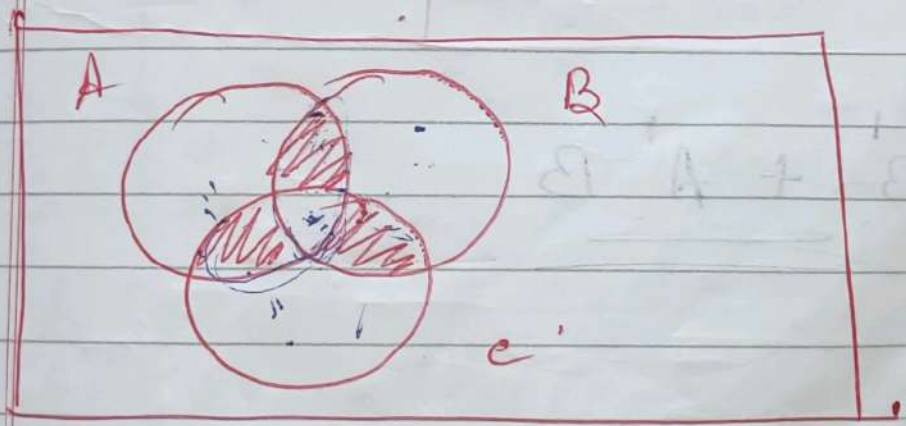


$X = A\bar{B}\bar{C} + AB\bar{C} + \bar{A}\bar{B}C$

$= A\bar{B}\bar{C} + \bar{B}C(A + \bar{A})$

$= A\bar{B}\bar{C} + \bar{B}C$

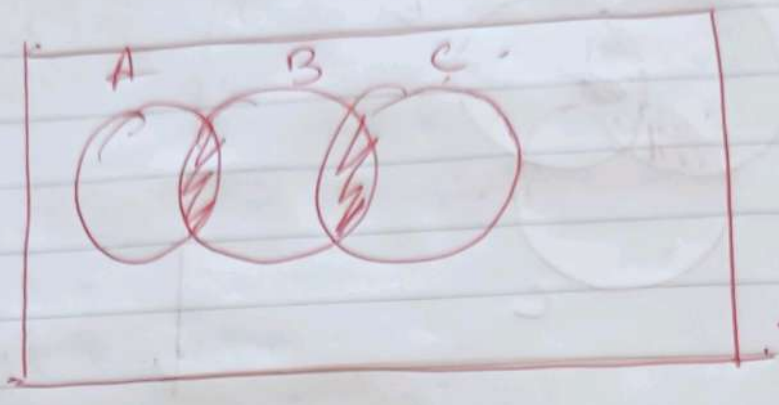
→ Write the Boolean exp for shaded area



$X = A\bar{B}\bar{C} +$

$X = AB'C' + AB'C + A'BC$

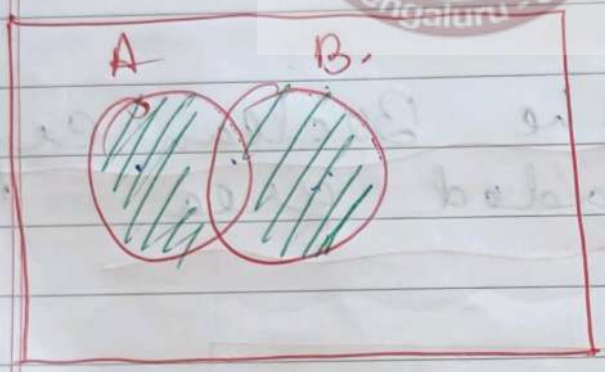
→ Write Boolean exp^{n} for shaded area:



$X = ABC' + A'BC$

→ Write Boolean exp for shaded area

(b)



$X = AB' + A'B$

→ Boolean functions :-

Boolean function is an expression formed with binary variables, two binary operators OR and AND and NOT, Parentheses and an equal 's sign.

Consider Boolean functions

$F_1 = xyz'$, $F_2 = x + y'z$,

$F_3 = x'y'z + x'yz + xy'$

$F_4 = xy' + x'z$

x	y	z	F_1	F_2	F_3	F_4
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	1	1	1
1	0	1	0	1	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	0

Any Boolean function is represented in form of truth table with 2^n combinations where n is num of variables in exp^n.

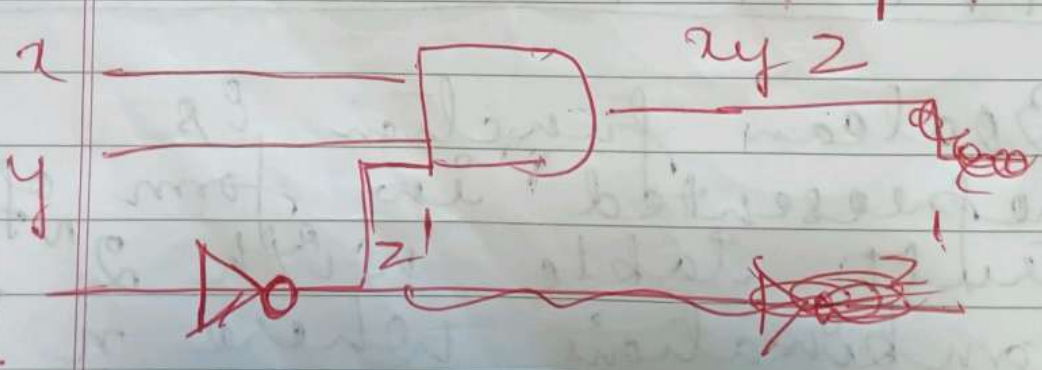
Boolean expression can be represented in logic diagram with the help of basic gates AND, OR and NOT.

Note: Simpler circuits can be obtained by manipulating the Boolean function.

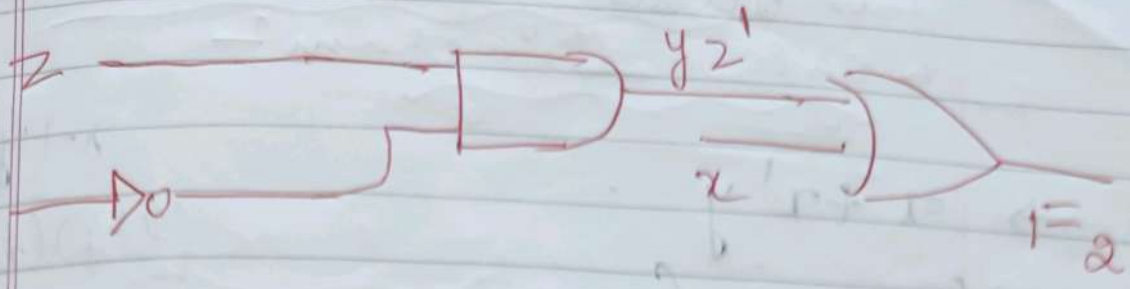
→ Literal: A literal is primed or unprimed variable. The number of literals in the Boolean exp can be minimized by algebraic manipulations.

→ Implementation of Boolean functions with Gates:

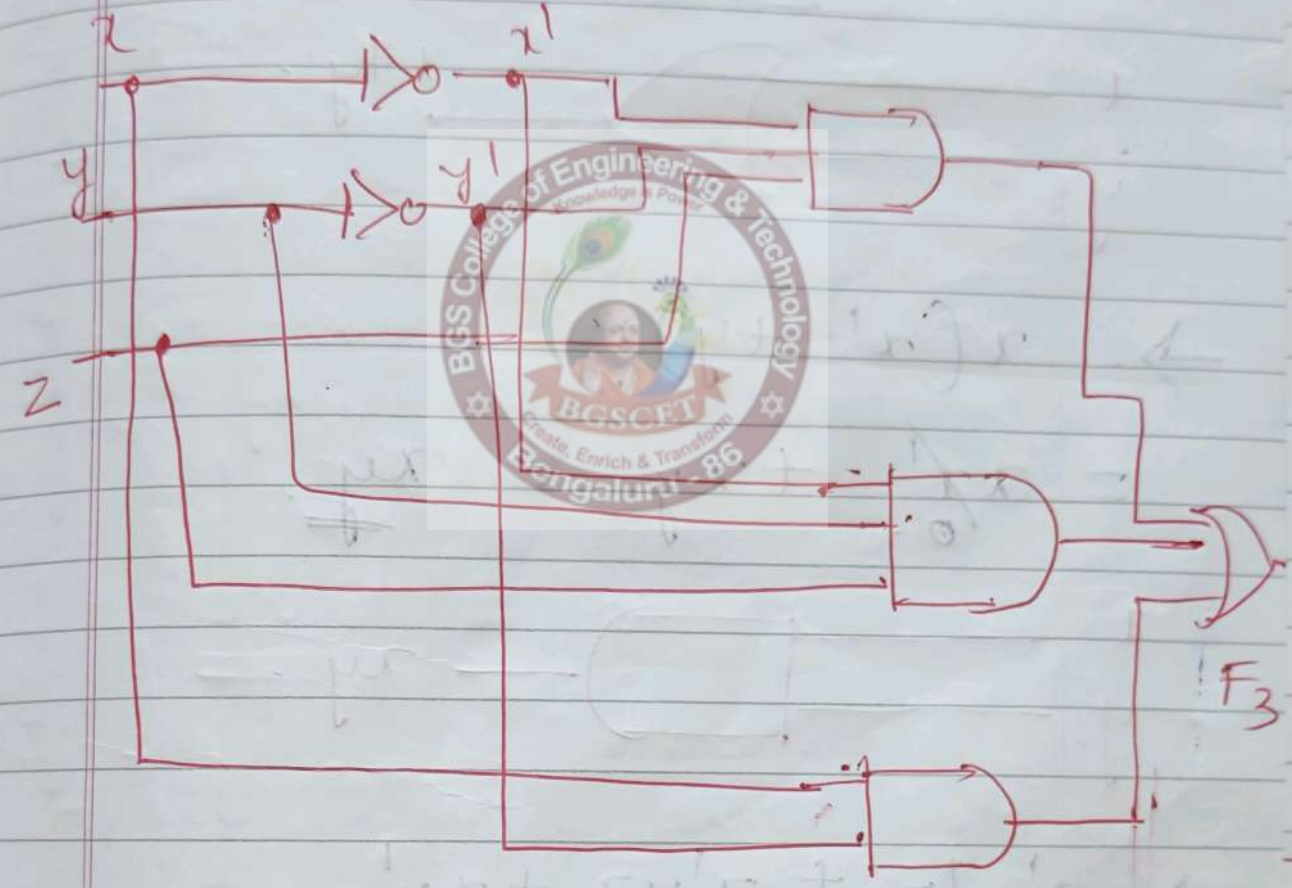
→ $F_1 = xyz'$



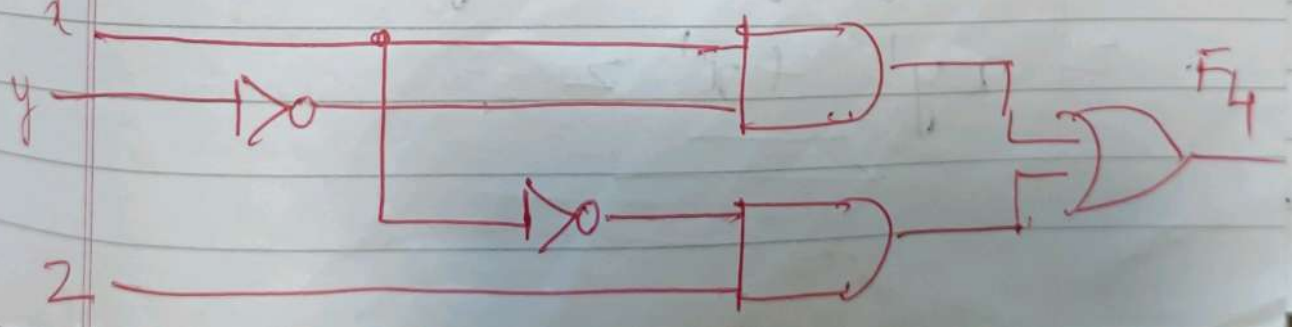
→ $F_2 = x + y'z$



→ $F_3 = x'y'z + x'yz + xy'$



→ $F_4 = xy' + x'z$



→ Simplify following Boolean functions and draw the logic diagram?

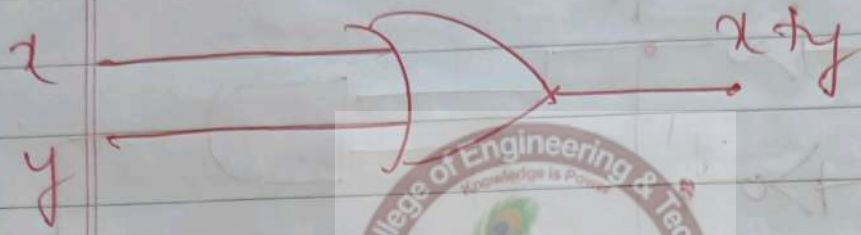
$x+yz$

$(x+y)(x+z)$.

→ $x+x'y$

$(x+x')(x+y)$

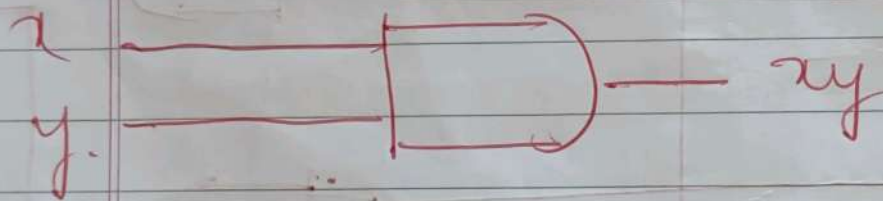
$= x+y$.



→ $x(x'+y)$

$= xx' + xy$

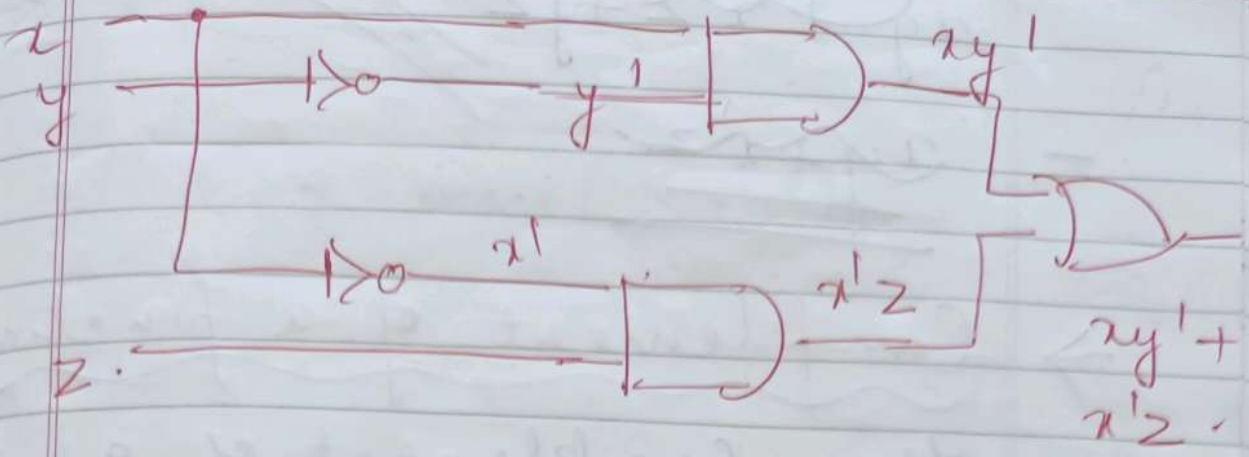
$= xy$.



→ $x'y'z + x'yz + xy'$

$x'z(y+y') + xy'$

$= xy' + x'z$.



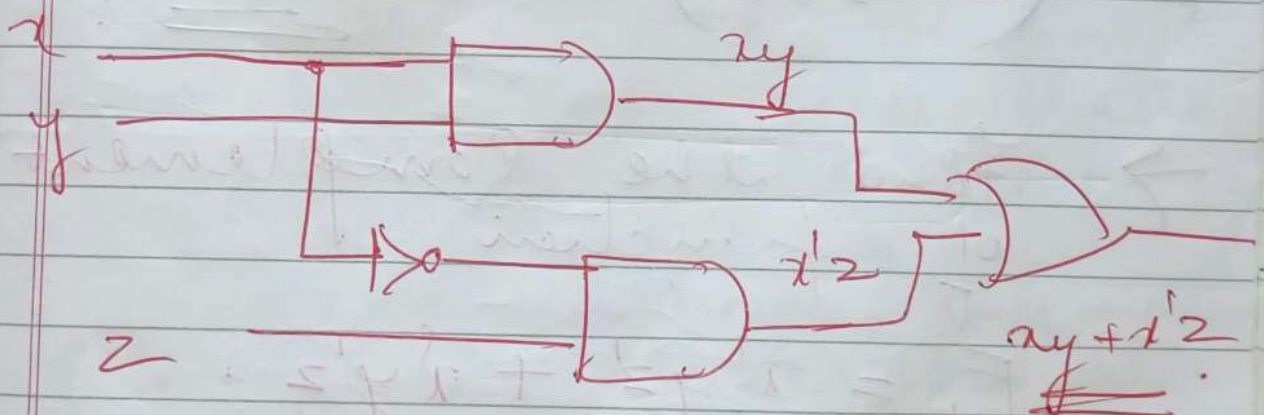
→ ~~xy~~ + x'z + yz

xy + x'z + yz(x+x')

= xy + x'z + xyz + x'yz.

xy(1+z) + x'z(1+y)

= xy + x'z :



→ (x+y)(x'+z)(y+z).

By applying Duality

x'y' + xz + y'z.

$xy + x'z + yz$

$= xy + x'z$

→ Complement of a function:

The complement of a function F is F'.
It is obtained by changing 0's to 1's & 1's to 0's.

DeMorgan theorem for complement state interchanging AND and OR operators & changing 1's to 0's & 0's to 1's.

$$(A + B + C)' = A' \cdot B' \cdot C'$$

→ Find the complement of function

$F_1 = x'yz' + x'y'z$

$F_1' = (x + y' + z) \cdot (x + y + z')$

$z[y + xy']$

$yy' + yz + y'z + xz \quad y_2' + y_2' x \cdot 1.$

→ $F_2 = x[y'z' + yz]$

$z[(y x)(y z)]$

$x' + (y + z) \cdot (y' + z')$

→ Find the Complement of

$x + x'y$

→ $x' \cdot (x + y')$

prove

$(x+y)(x+z) = x + yz$

$xy + xz + yz' = xz + yz'$

→ Canonical And Standard form:-

→ Min Terms:-

Two binary variables x and y combined with AND operation. This may have 4 possible combinations $x'y$, xy', $x'y'$ & xy.

Each of these four AND terms are called Min terms or a Standard Product.

If there are n variables they can be combined to form

2^n minterms. It will from 0 to $2^n - 1$.
Each minterm is obtained from an AND term of n variables with each variable being primed (x') of bit is 0 & a unprimed (x) of bit is 1.

→ Min term for three Binary Variables

x	y	z	Term	Min terms Designation
0	0	0	$x'y'z'$	m_0
0	0	1	$x'y'z$	m_1
0	1	0	$x'yz'$	m_2
0	1	1	$x'yz$	m_3
1	0	0	$xy'z'$	m_4
1	0	1	$xy'z$	m_5
1	1	0	xyz'	m_6
1	1	1	xyz	m_7

→ Max Terms:-

Max term is obtained from an OR term of n variable with each variable primed (x') of bit is 1.

(a).

and unprimed if bit is 0.
Each Maxterm is complement of minterm & vice versa.

→ Max terms for three Binary Variables

x	y	z	Term	Max terms Designation	
0	0	0	$x+y+z$	M_0	0
0	0	1	$x+y+z'$	M_1	1
0	1	0	$x+y'+z$	M_2	1
0	1	1	$x+y'+z'$	M_3	0
1	0	0	$x'+y+z$	M_4	1
1	0	1	$x'+y+z'$	M_5	0
1	1	0	$x'+y'+z$	M_6	0
1	1	1	$x'+y'+z'$	M_7	1

& Max

→ Max terms for Two Binary Variables.

x	y	Minterm Term		Designation	Maxterm	
0	0	$x'y'$	0	m_0	$x+y$	M_0 0
0	1	$x'y$	0	m_1	$x+y'$	M_1 1
1	0	xy'	0	m_2	$x'+y$	M_2 1
1	1	xy	1	m_3	$x'+y'$	M_3 1

$(x+y')(x'+y')$
$M_1 M_3$

$x'y' + x'y + xy' + xy$

→ To write function for Min terms?

using truth table, form min terms that produces 1 for a function.

$f_1 = x'y' + xy$

$= 01 + 11$

$= 0 + 1 = 1$

$f = f_1$ function is

Sum of product (SOP) form. product of variables are ored.

Ily another combination

$f_2 = x'y' + xy$

$= 1$

Min term are represented by Σ

$f_1 = \Sigma(m_0, m_3)$ $\Sigma m(m_0, m_3)$

$\Sigma m(1, 3)$

$f_2 = \Sigma(m_0, m_3)$

→ To write function for Max term using truth table form max term that produces '0' in a function.

OR

By applying duality to min term function.

$f_1 = (x+y)(x+y') = 0$.

Max term represented by $\overline{11}$

$f_1 = \Pi(M_0, M_3)$

$f_1 = (x+y)(x+y) = 0$.

Max term represented by $\overline{11}$.

$\Pi(M_2, M_0)$

$f_2 = (x+y')(x+y) = 0$.

$\Pi(M_1, M_0)$

→ Function for Min Terms (three Variables)

$f_1 = x'y'z + xy'z' + xyz$

$\Rightarrow f_1 = m_1 + m_4 + m_7$

$\Rightarrow f_1 = \Sigma(m_1, m_4, m_7)$

Another combination.

$f_2 = x'yz' + xy'z + xyz$

$\Rightarrow f_2 = \Sigma(m_2, m_5, m_7)$

→ Function for Max terms (three variables)

$f_1 = (x'+y'+z)(x+y'+z')(x+y+z)$

$M_6 \quad M_3 \quad M_0$

$\Pi(M_0 M_3 M_6)$

$f_2 = (x'+y+z')(x+y'+z)(x+y+z)$

$\Pi(M_5 M_2 M_0)$

Another Combination.

$f_2 = x'yz + xy'z + xyz' + xyz$

$= m_3 + m_5 + m_6 + m_7 = 1.$

⇒ Functions for Max term (three Variable)

Form minterm for each combination that produces 0 in the function and then ORing the terms

$f_1 = x'y'z' + x'yz' + x'yz + xy'z + xy'z'$

Complement f_1

$f_1 = (x+y+z)\,(x+y'+z)\,(x+y'+z')\,(x'+y+z')\,(x'+y'+z).$

$= M_0 M_2 M_3 M_5 M_6.$

Similarly.

$f_2 = (x+y+z)\,(x+y+z')\,(x'+y+z)$

$(M_0 M_1 M_4)$

Imp Note: Boolean functions expressed as sum of minterms or product of maxterms are called Canonical form.

→ To represent Boolean function as Sum of Minterms

The minterms in the function are those that give 1's.

Boolean function can be expressed in form of sum of Minterms by the following steps.

→ If the term misses any of the variables it is ANDED with an expression ex: $(x+x')$.

→ Express Boolean function $F = A + B'C$ in Sum of Minterms

$F = A + B'C$.

→ Take first term A. missing two variables B & C.

$F = A(B+B') = AB + AB'$.

Still C is missing.

$AB(C+C') + AB'(C+C')$.

$= ABC + ABC' + AB'C + AB'C'$.

Take II nd term $B'C$.

A is missing

$B'C = B'C(A+A')$.

$= AB'C + A'B'C$.

Combining all terms

$F = ABC + ABC' + AB'C + AB'C' + AB'C + A'B'C$.

$F = A'B'C + AB'C' + AB'C + ABC' + ABC$.

$F = m_1 + m_4 + m_5 + m_6 + m_7$.

$F(A,B,C) = \Sigma(1,4,5,6,7)$.

→ Truth Table for $F = A + B'C$.

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

From the truth table Sum of minterms

$F = A'B'C + AB'C' + AB'C + ABC' + ABC$

$F = \Sigma(1, 4, 5, 6, 7)$

→ To Represent Boolean function as product of Max Terms.

→ By using Distributive Law $x + yz = (x + y)(x + z)$.

→ Any missing Variable in each term is ORED with xx'.

$(A+B+C')$ $(A'+B+C)$ $(A'+B+C')$ $(A+B'+C)$ $(A+B'+C')$.

→ Express Boolean function $f = xy + x'z$ in product of maxterm form.

$f = xy + x'z$

$= (xy + x')(xy + z)$

$x + yz$

$(x+y)(x+z)$.

$(x'+x)(x'+y)(x+z)(y+z)$

$(x+y)$

$F = (x'+y)(x+z)(y+z)$.

$x'+y$ missing z.

$x'+y+(zz') = (x'+y+z)(x'+y+z')$

$x+z+(yy') = (x+z+y)(x+z+y')$.

$y+z+(xx') = (x+y+z)(x'+y+z)$.

Combining all terms.

$F = (x+y+z)(x+y'+z)(x'+y+z)(x'+y+z')$

$f = M_0 M_2 M_4 M_5$

$f(x, y, z) = \Pi(0, 2, 4, 8)$

→ Conversion Between Canonical forms

Consider function with min terms

$F(A, B, C) = \Sigma(1, 4, 5, 6, 7)$

$F'(A, B, C) = \Sigma(0, 2, 3)$

$= M_0 + M_2 + M_3$

$F = (M_0 + M_2 + M_3)'$

$= M_0' \cdot M_2' \cdot M_3'$

$M_0 M_2 M_3$

$f = \Pi(M_0 M_2 M_3)$ → Product of Max terms

Note: $m_j' = M_j$ m_j

$\Sigma(1, 3, 7)$ $(x'y'z + x'yz + xyz)'$

$x=y$ $(x+y+z')$ $(x+y'+z)$ $(x+y'+z')$

(001) (010) (011) (100)

→ To find Maxterms from Truth table for function $F = xy + x'z$

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$(x+y+z)$

From truth table max term are

M_0, M_2, M_4, M_5

$F = \Pi(M_0, M_2, M_4, M_5)$

→ **Standard forms:-**

Boolean functions are expressed in Standard forms. There are two types of Standard forms.

→ Sum of product

→ product of Sum.

Sum of product contains AND terms called product terms & these product terms are ORED

Ex: $F_1 = xy' + xz + x'y$.

Product of Sum contains sum of literals and these are ANDED.

ex: $F_2 = (x+y+z')(x+y'+z)$.

Some Boolean exp^{n} are expressed in Non-standard form.

$F_3 = (AB+CD)(A'B+CD)$.

Such expression have to be changed to standard form.

P.T $xy + xz + yz' = xz + yz'$.

$xy(z+z') + xz + yz'$

$xyz + xyz' + xz + yz'$

$xz + yz'(1+x)$

$= xz + yz'$

Other Logic Operations:

Boolean expressions and Symbols for 16 functions for two variables.

$F_0 = 0$.	Null.	
$F_1 = xy$.	AND. $x \cdot y$.	
$F_2 = xy'$	x/y.	
$F_3 = x$.		
$F_4 = x'y$	y/x.	
$F_5 = y$.		
$F_6 = xy' + x'y$.	$x \oplus y$	EXOR.
$F_7 = x + y$.	$x + y$	OR.
$F_8 = (x+y)'$	NOR $x \downarrow y$.	NOTOR
$F_9 = xy + x'y'$	$x \odot y$.	EXNOR.
$F_{10} = y'$	y'	
$F_{11} = x + y'$.	$x \subset y$.	

$F_{12} = x'$

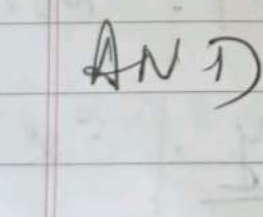
$F_{13} = x' + y$ | $x \supset y$.

$F_{14} = (xy)'$ | $x \uparrow y$ | NAND not AND

$F_{15} = 1$.

→ Digital Logic Gates

Boolean Algebra functions are expressed in terms of AND, NOT and OR. Other gates are Not AND & NAND.
NOT OR - NOR.
EXOR
EXNOR.

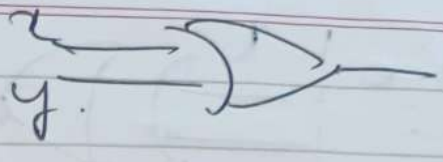
Name	Symbol	Function	TT		
			x	y	xy
AND		xy	0	0	0
			0	1	0
			1	0	0
			1	1	1

classmate

Date

Page

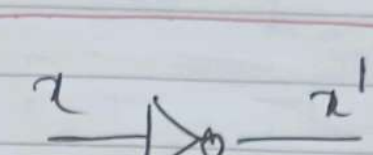
OR.



$x + y$

x	y	x+y
0	0	0
0	1	1
1	0	1
1	1	1

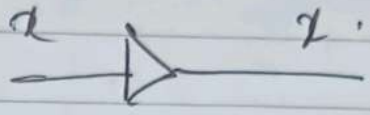
NOT (Inverter)



x'

x	x'
0	1
1	0

Buffer



x

x	F
0	0
1	1

NAND.

$(xy)'$

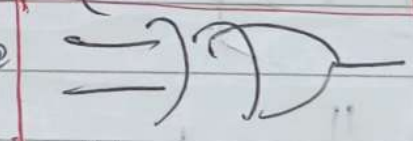
x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

NOR.

$(x+y)'$

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

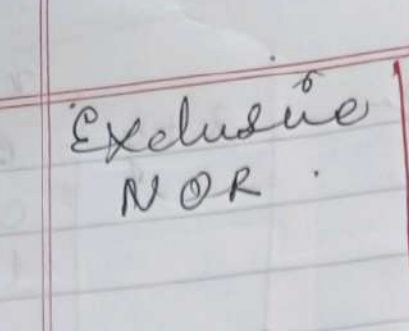
Exclusive OR.



$x'y + xy'$

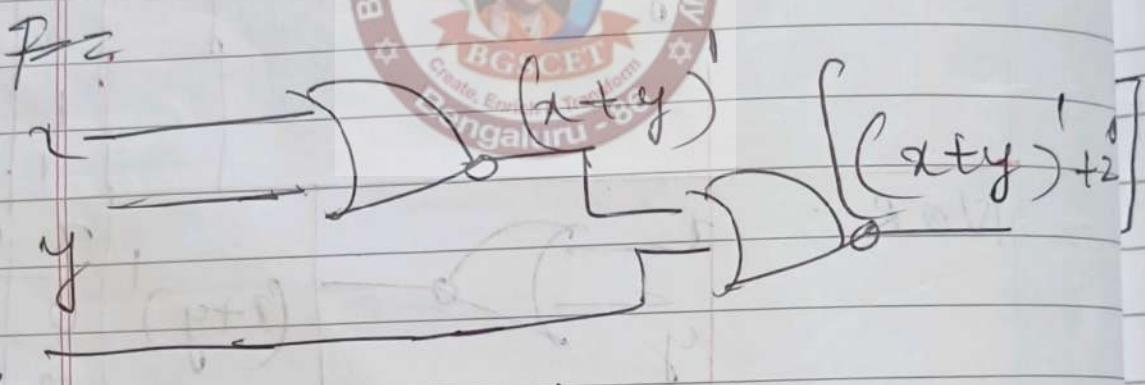
x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive NOR



x	y	F
0	0	1
0	1	0
1	0	0
1	1	1

→ Extension To Multiple Inputs :-

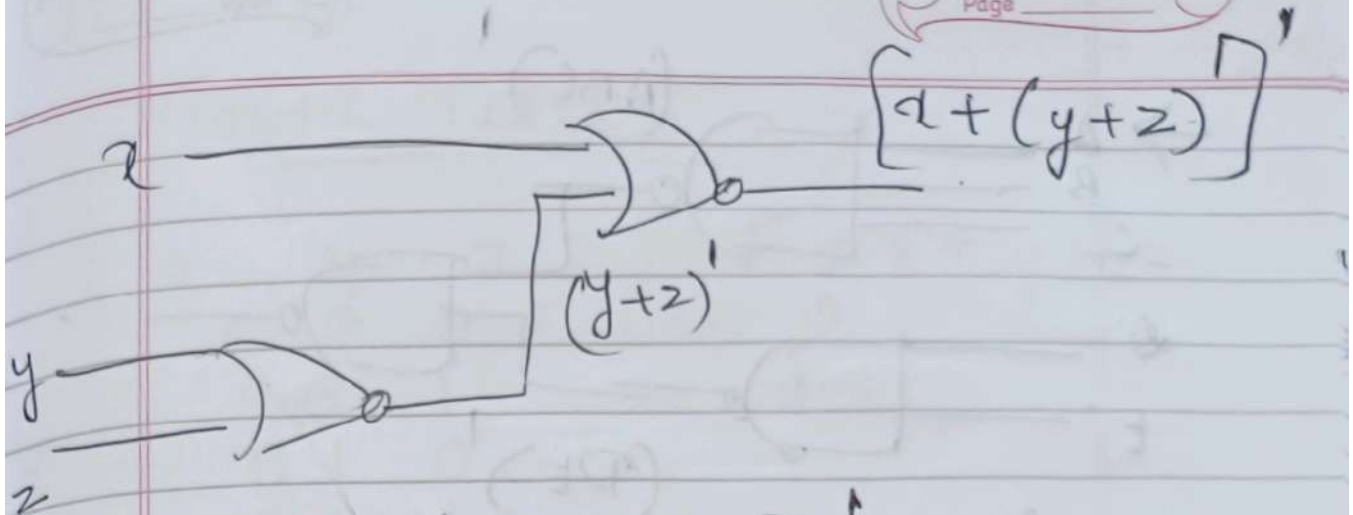


$$F = \left[(x+y)' + z\right]'$$

$$F = (x+y)'' \cdot z'$$

$$= (x+y)\,z'$$

$$F = xz' + yz'$$



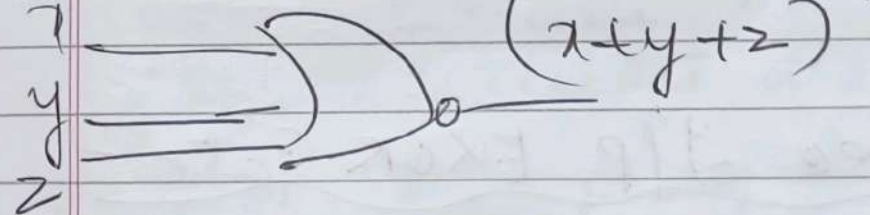
$$F = [x + (y+z)']'$$

$$F = x' \cdot (y+z)''$$

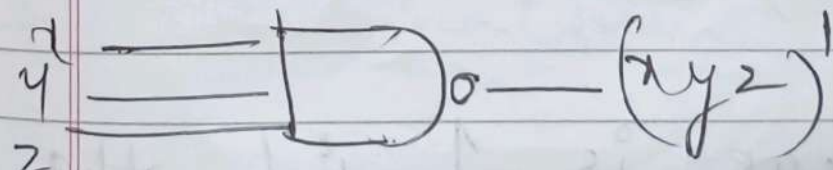
$$F = x'(y+z)$$

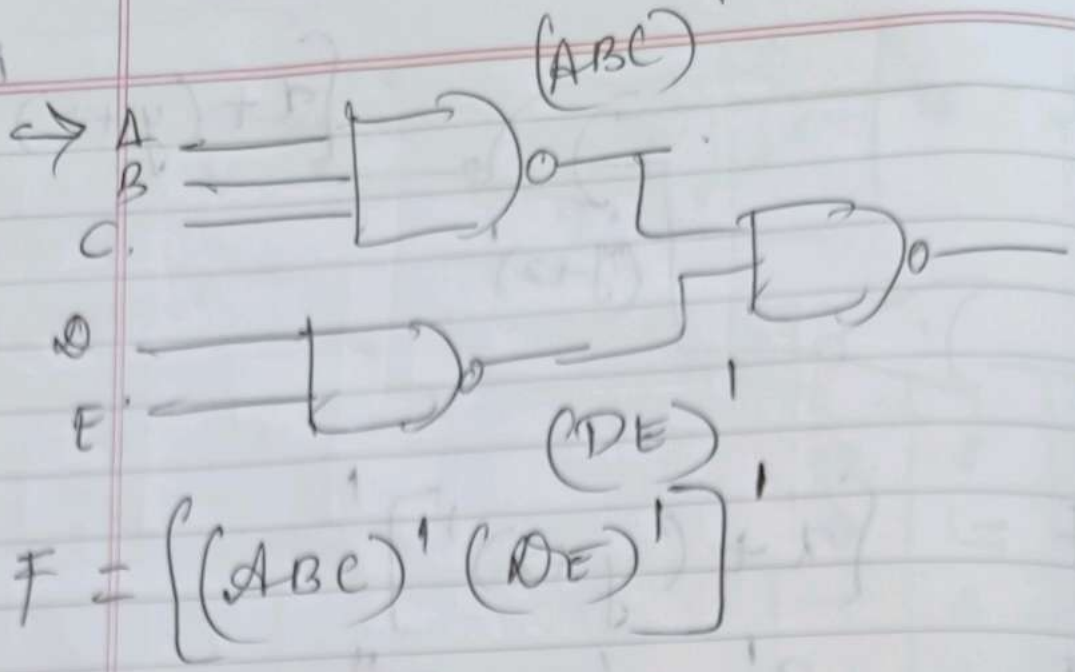
$$F = x'y + x'z$$

→ Three i/p NOR Gate :-



→ Three i/p NAND Gate :-

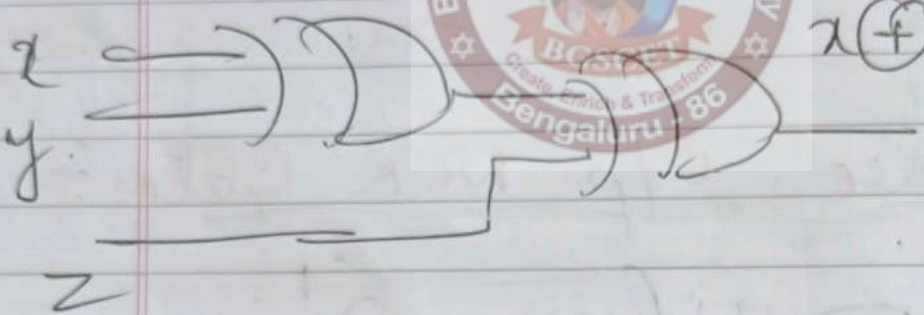




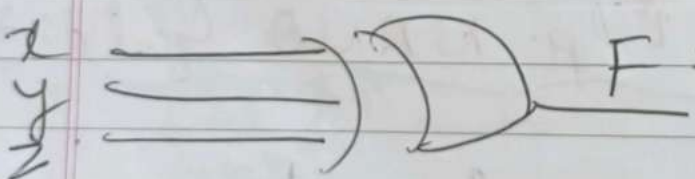
$$F = [(ABC)'(DE)']'$$

$$F = ABC + DE$$

→ Two I/P EXOR Gate



→ Three I/P EXOR Gate :



o/p of EXOR is 1 if the i/p variable have an odd number of 1's

Truth Table

x	y	z	$F = x \oplus y \oplus z$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

→ Combinational Logic:

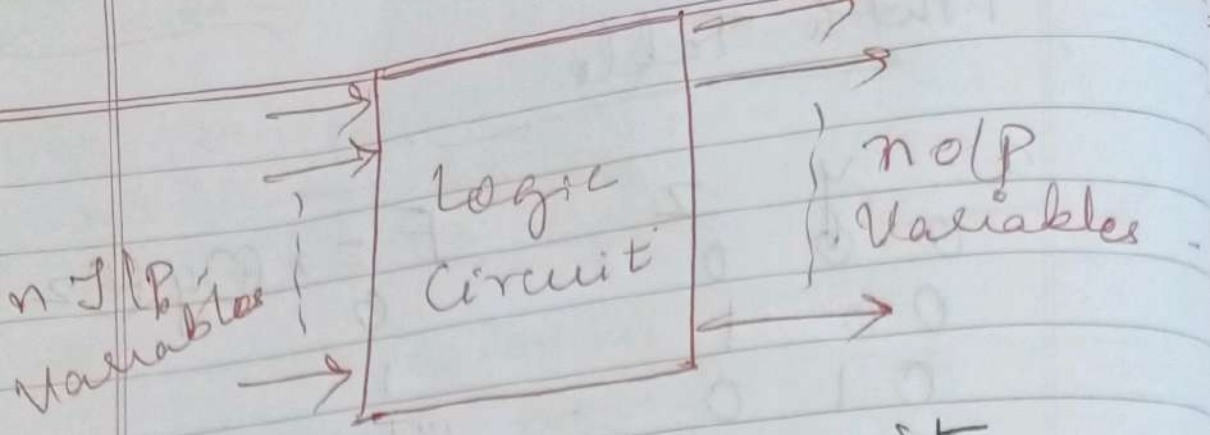
Digital logic gates are used to perform specific operations in Boolean Algebra. These are called digital logic circuits.

Logic circuits are of two types

→ Combinational

→ Sequential.

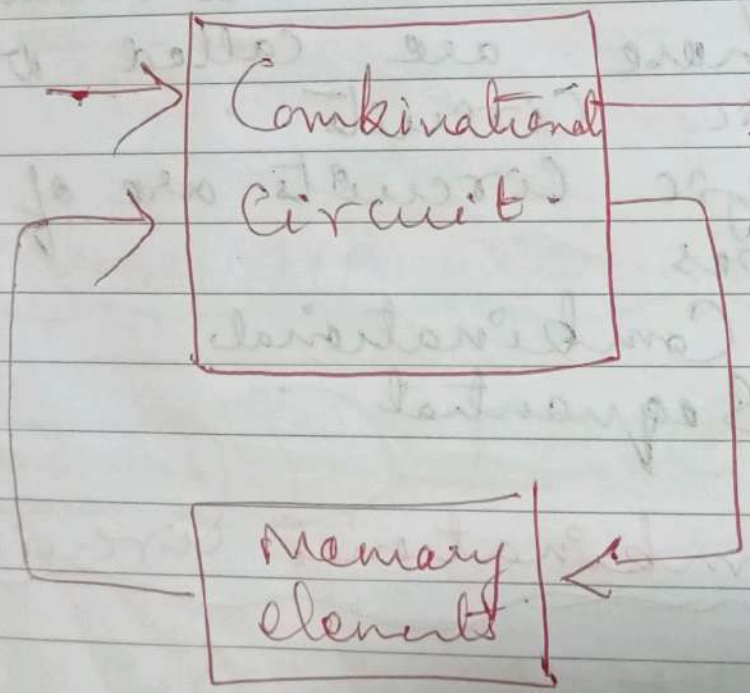
→ Combinational Circuit:-



→ Combinational circuit consists of I/p variables, logic gates and O/P variables.

→ O/p is determined from present combinations of I/p's without depending on previous I/p's.

→ Sequential Circuits :-



→ Sequential circuit consists of series of I/P's & O/P's.
→ The O/P of sequential circuit depends on both present & previous O/P's.
→ Sequential circuit consists of Memory element.

→ Difference Btw Combinational & Sequential Circuit

Combinational	Sequential
→ O/P depend only on present I/P	O/P depends on present & previous I/P & previous O/P.
→ feed back is not present	feed back is present.
→ Memory elements not required	memory elements are used.
→ Simple to design.	Design is complex.

→ Design of Combinational Circuits :-

The design procedure of combinational circuit

Involves following steps.
→ Problem is stated
→ Number of available I/P variables and O/P are determined
→ I/P and O/P variables are assigned letter symbols.
→ Truth table that defines relation b/w I/P's and O/P's are derived
→ Simplified Boolean function is obtained
→ Logic diagram is drawn.

A practical design method would consider following Constraints.
→ Minimum number of gates
→ Minimum number of I/P's to a gate.
→ Minimum number of interconnections

→ Adders:

Digital Computers perform various tasks among which arithmetic operation

are basic tasks.
Addition of two binary digits is an example.

→ Half Adder:-

Half Adder circuit adds two binary digits and produces two O/P's valued Sum and Carry.

Truth Table

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

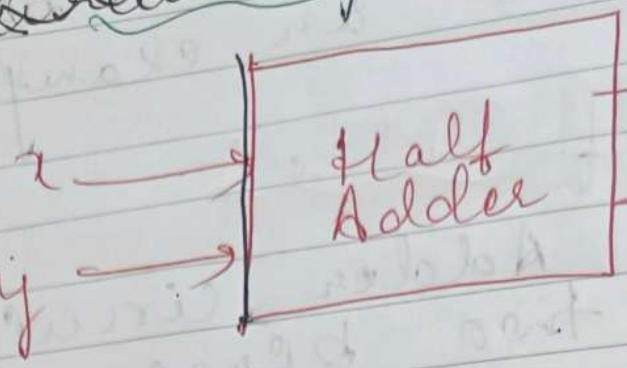
Half Adder has 2 I/P's x and y and two O/P's Sum and Carry. It performs binary addition of x and y.

From the truth table expression for Sum and Carry are

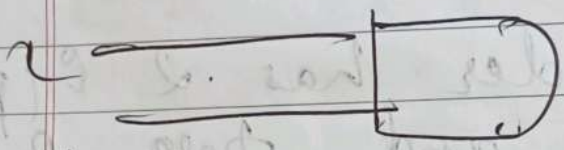
$S = x'y + xy' = x \oplus y$.

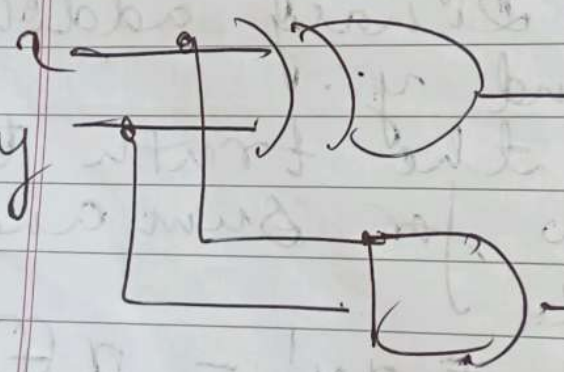
$C = xy$.

The Combinational diagram circuit for Half Adder:



Combinational Logic diagram





Implementation of Half Adder

$S = x'y + xy'$ $C = xy$.

$S = x'y + xy'$

This is in sum of product form.

To implement in product of sum form.

$S = (x+y)(x'+y')$.

→ Full Adder:-

Full adder is a combinational circuit that adds 3 i/p variables or bits and produces two o/p's. Sum and Carry.

x	y	z	Sum	Carry.
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The expression for Sum from the truth table is

$S = x'y'z + x'yz' + xy'z' + xyz$

The expression for carry using truth table

$C = x'yz + xy'z + xyz' + xyz$

$C = yz(x+x') +$

$C = x'yz + xy'z + xy(z+z')$

$C = x'yz + xy'z + xy$

$C = x'yz + x(y+y'z)$

$x+x'y = x+y$

$C = x'yz + x(y+z)$

$C = x'yz + xy + xz$

$C = y(x'z + z) + xz$

$C = y(x+z) + xz$

$C = xy + yz + xz$

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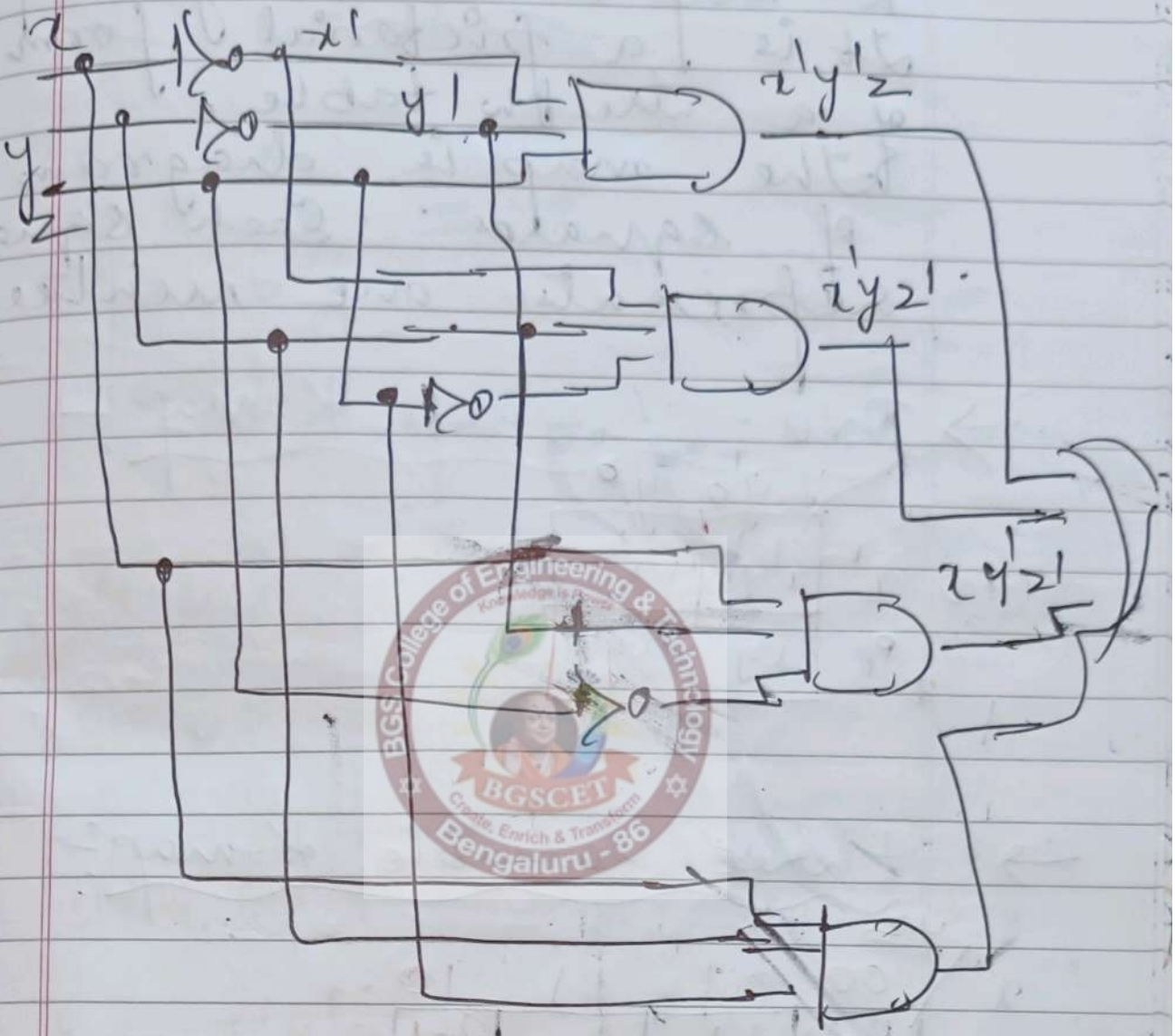
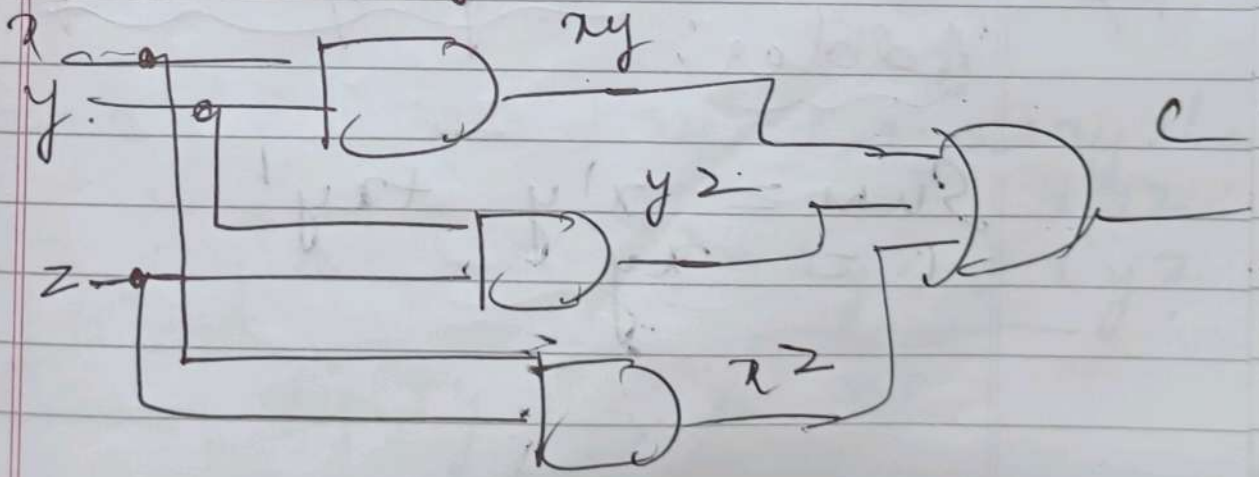
Implementation using Logic Diagram for Sum



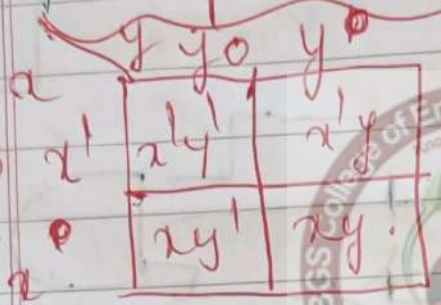
For carry :-



→ Concept of K-map:-

K-map is Karnaugh map. It is a pictorial form of a truth table. The map is diagram of squares. Each square represents one minterm.

→ Two-Variable K-map:-



→ three Variable K-map:-

x \ yz	00	01	11	10
0	x'y'z'	x'y'z	x'yz	x'yz'
1	xy'z'	xy'z	xyz	xyz'

→ Draw K-map for Half Adder:

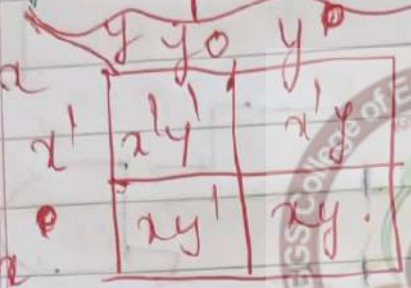
Sum = x'y + xy'

C = xy

→ Concept of K-map:-

K-map is Karnaugh map. It is a pictorial form of a truth table. The map is diagram of squares. Each square represents one minterm.

→ Two-Variable K-map:-



→ Three Variable K-map:-

x \ yz	00	01	11	10
0	x'y'z'	x'y'z	x'yz	x'yz'
1	xy'z'	xy'z	xyz	xyz'

→ Draw K-map for Half Adder:

Sum = x'y + xy'

C = xy

x \ y	0	1
0	0	1
1	1	0

$S = xy' + x'y$

x \ y	0	1
0	0	0
1	0	1

$C = xy$

→ 1. Draw K-Map for full Adder.

x \ yz	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$S = x'y'z + xy'z' + x'yz' + xyz'$.

x \ yz	00	01	11	10
0		1	1	
1	1		1	1

$C = xy'z + xyz + xy'z + xyz + xyz' + x'yz$.

$C = xy'z + xyz' + xyz + x'yz$.

$C = xy + yz + xz$

→ Implement Full Adder using two Half Adders an OR Gate:-

Expression for Sum of full adder is

$S = x'y'z + x'yz' + xy'z' + xyz$

and

$C = x'yz + xy'z + xyz' + xyz$

$S = x'(y'z + yz') + x(y'z' + yz)$

$S = x'(y \oplus z) + x(y \oplus z)'$

let $y \oplus z = y$

$S = x'y + xy'$

$S = x \oplus y$

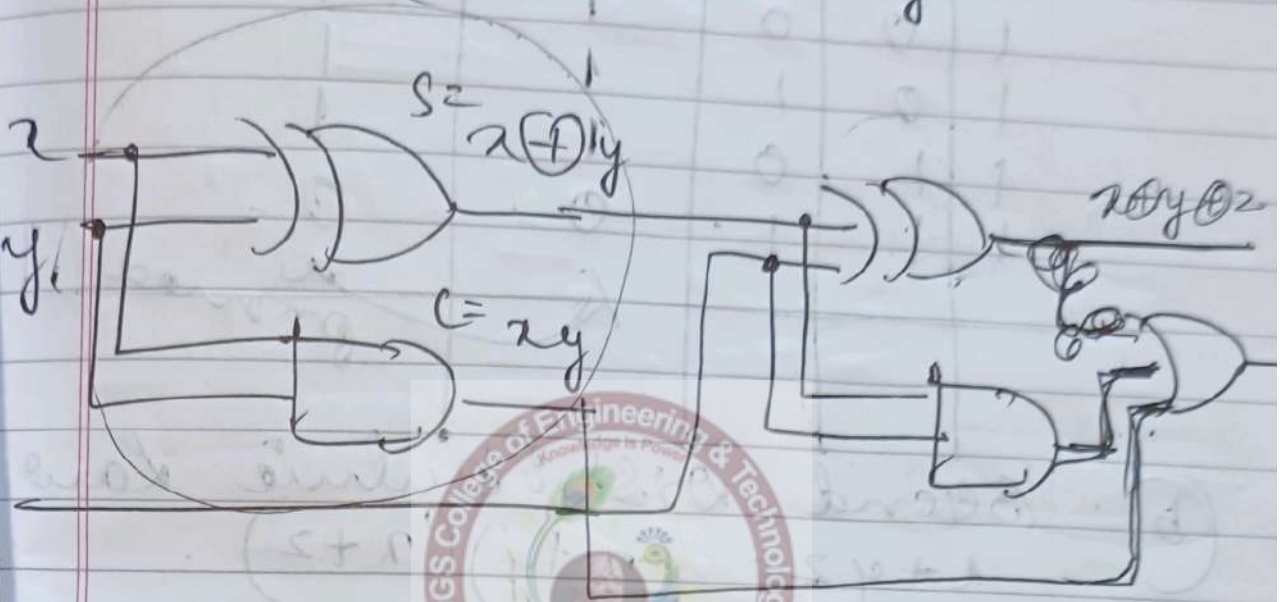
$S = x' ($

$S = x \oplus y \oplus z$

HA1

HA2

$$C = x'yz + xy'z + xyz' + xyz$$
$$C = z(x'y + xy') + xy(z + z')$$
$$C = z(x \oplus y) + xy$$



Problems:-

Demonstrate by means of truth table the validity of following Identities

(a) Demorgans theorem for $(xyz)' = x' + y' + z'$

x	y	z	$(xyz)'$	$x'+y'+z'$
0	0	0	1	1
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	0	0
1	1	1	0	0

proved

(b). Second Distributive Law

$x+yz = (x+y)(x+z)$

x	y	z	$(x+y)$	$(x+z)$	$x+yz$	$(x+y)(x+z)$
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	1	0	0	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

proved

(c). $xy + x'z + yz$

$xy + x'z + yz(x+x')$

$xy + x'z + xyz + x'yz$

$xy(1+z) + x'z(1+y)$

$xy + x'z$ proved.

→ Simplify the Boolean expressions to minimum num of literals

① $x'y' + xy + x'y$

$= x'(y'+y) + xy$

$= x' + xy$.

$x'y' + y(x+x')$

$y + x'y'$

$(y+x')(y+x')$.

$(x+y)(x+z)$
0
0
0
1
1
1
1

proved

② $(x+y)(x+y')$

$xx + xy' + xy + yy'$

$x + xy' + xy$.

$x(1+y') + xy$.

$x + xy$

$x(1+y) = x$

(3) $x'y + xy' + xy + x'y'$

$x'(y+y') + x(y+y')$

$= x' + x = 1$

(4) $x' + xy + xz' + x'y'z'$

$x' + xy + xz'(1+y')$

$x' + xy + xz'$

(5) $xy' + y'z + x'z'$

$xy' + y'z + x'z'$

$xy' + y'z(x+x') + x'z'$

$xy' + xy'z + x'y'z + x'z'$

$xy'(1+z) + x'y'z + x'z'$

$xy' + xy'z + x'z'$

$xy'(1+z) + x'z'$

$xy' + x'z'$

(6) $ABC + A'B + AB C'$

$AB(C + C') + A'B$

$= AB + A'B$

$B(A + A') = B$

(7) $x'yz + xz$

$x'yz + xz(y + y')$

$x'yz + xyz + xy'z$

$yz(x + x') + xy'z$

$yz + xy'z$

$y z(z(y + xy')$

$z(x + y)$

xyz

$x(yz)$

$x + yz$

$(x+y)(x+z)$

→ Reduce the Boolean expressions as indicated

$A'C' + ABC + AC' \rightarrow$ 3 literals

$C'(A + A') + ABC$

$C' + ABC \rightarrow AB(C + C')$

$= AB$

(2) $(x'y' + z)' + z + xy + wz$ up to 3 literals

$(x'y' \cdot z)' + z + xy + wz$

$(x+y) \cdot z') + z + xy + wz$

$(x+y)z' + z + xy + wz$

$xz' + yz' + z + xy + wz$.

$xz' + yz' + xy + w$.

$xz' + y(z + z') + w$

$xz' + xyz' + xyz + xyz' + w$

$xz' + xy + xyz + w$.

$xz' + z + w$.

$x(z + z') + w = x + w$.

→ Find the Complement of $F = x + yz$

(1) $(x + yz)' = x' \cdot (y' + z')$.

(2) $xy' + x'y$

$(xy' + x'y)'$

$(x' + y) \cdot (x + y')$

(3) $(AB' + C)D' + E$

$[(AB' + C)D' + E]'$

$(A' + B) \cdot C + D \cdot E$

(4) $(x + y' + z)(x' + z')(x + y)$

$(x' \cdot y \cdot z') + (x \cdot z) + (x' \cdot y')$

→ Use Demorgans theorem convert the Boolean exp^{n} that have only OR & Complement operation.

$F = x'y' + x'z + y'z$

$F = x'y' + z'z + y'z$

use Demorgans theorem for each term

$F = (x'y')' + (x'z)' + (y'z)'$

$= \overline{x} + y + \overline{z} + z' + y' + z'$

$= x + y + y' + z'$

$= x + 1 + z'$

$= 1$

use DeMorgans theorem for the expression so that it contains only AND and NOT Gates:

$F = (y + z')(x + y)(y' + z)$

$= (y + z')'(x + y)'(y' + z)'$

$= (y'z)(x'y')(yz')$

$= (y'z)(x'y')(yz')$

$F = x'y' + x'z + y'z$

Take Complement

$F = (x'y' + x'z + y'z)'$

$(x'y')' \cdot (x'z)' \cdot (y'z')'$

→ Obtain truth table and expression as Sum of min terms and product of max terms:

① $(xy + z)(y + xz)$

x	y	z	$(xy+z)$	$(y+xz)$		O/P
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

Sum of Min terms

xyz ~~$+ x'y'z' +$~~

~~$+$~~

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Module-4 Embedded Systems

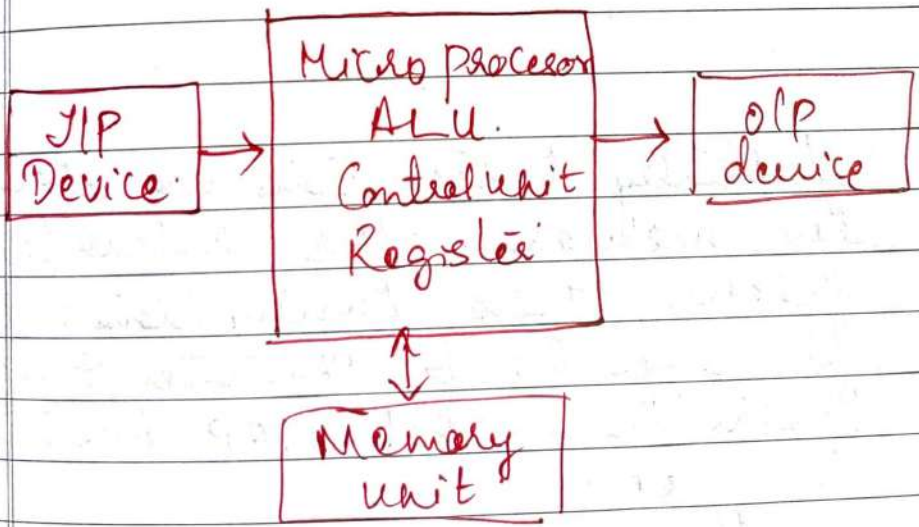
Microprocessor:-

Computers Central Processing unit (CPU) built on a single Integrated chip is called a Micro processor.

A digital Computer with one microprocessor is called Micro Computer.

Microprocessor contains millions of tiny components like transistors, resistors and diodes that work together.

Block Diagram of Micro Processor:



Microprocessor consists of Arithmetic and logic unit (ALU), Control unit and registers.

ALU performs arithmetic and logic operations on data received from an i/p device or memory.

Control unit controls the instructions within the computer.

Register used to store the data.

Fourth Generation Microprocessor:

32-bit microprocessors were introduced ex: Intel 80386.

Fifth Generation Microprocessor:

64-bit microprocessors were introduced.

Working of Microprocessor:

Initially instructions are stored in memory. The microprocessor fetches these instructions & decodes it & executes these instructions till STOP instruction is met.

Then it sends result in binary form to the output.

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→ **Micro Controller :-**

A micro controller is a small & low cost micro computer designed to perform specific tasks of the system like micro wave information, receiving remote signals.

General Micro Controller consists of processor, memory, serial ports, peripherals (timers, counters).

→ **Microprocessor Vs Micro Controller**

Microprocessor	Micro Controller
(1) Consists of CPU, ALU.	Highly integrated chip contains CPU, memory, I/O ports.
Ex: Intel 8086.	Ex: Intel 8051.
(2) Used in personal computers	used in Embedded Systems
(3) Dependent unit	Self Contained unit
(4) Limited power saving options	Includes lot of options.
(5) Consumes more power	Consumes less power.

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→ Define Embedded System with an example.

An Embedded System is a microcontroller or microprocessor based system which is designed to perform specific tasks in combination of both hardware & software.

Ex:- Electronic toys, Mobile handsets, washing machines, Air Conditioner, DVD player, Set top box.

fire alarm sense only smoke. Laser printer prints.

Note:- Firmware:- programming instructions stored in read-only memory (ROM).

→ Embedded System V/s General Computing System:

General Computing S/m.	Embedded S/m.
(1). Made processor based S/m.	Micro Controller based S/m.
(2). Computer need human Interaction to perform tasks	Embedded device does not need human Interaction to perform tasks.

General Computing S/m.	Embedded S/m.
(3) Power Consumption is high	power Consumption is less.
(4) Harvard / Von Neumann architecture	Medium Scale Embedded S/m. Harvard architecture.
(5) Reduced Instruction Set Computer	Complex Embedded S/m.
(6) It has 2 parts Hardware and Software	3 parts hardware software and firmware.

RISC V/s CISC.

RISC: Reduced Instruction Set Computer.
CISC: Complex Instruction Set Computer.

They are two types of Computer architectures that are used to design microprocessor found in computers. They are used to enhance performance of CPU.

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RISC architecture has small set of instructions
CISC architecture has set of large number of instructions.

	RISC	CISC.
(1)	Reduced Instruction set Computer	Complex Instruction set Computer.
(2)	Simple decoding of instructions	Complex decoding of instructions.
(3)	~~Length of code is short.~~	
(3)	Small Code size	Large code size.
(4)	Less Execution time	More execution time
(5)	RISC used in Micro processor	used in Micro Controller.
(6)	Software Centric Design	Hardware Centric Design.
(7)	uses Harvard architecture	uses Vonneumann architecture / Harv
Ex:	IBM RS6000.	Ex: Intel 386. Intel 486, Pen

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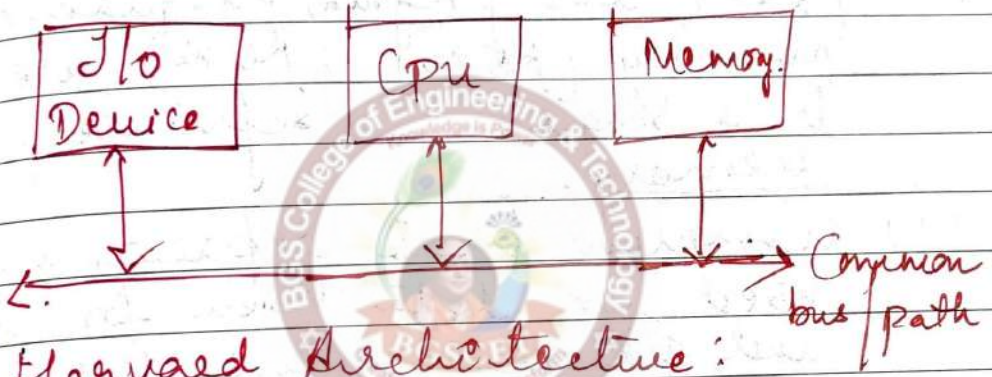
Micro Controller Architecture :

Micro Controller architecture are two types :
1. Von - Neumann.
2. Harvard.

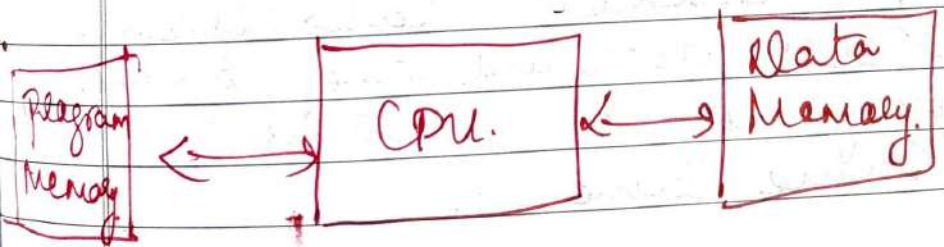
Von-Neumann Architecture :

In this architecture program & data instructions are stored in same memory.



Harvard Architecture :

In this architecture separate memory is used for storing program and data instructions.



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Von-Neumann V/s Harvard Architecture:

	Von-Neumann.	Harvard.
(1).	Ancient Computer architecture based model.	Modern Computer architecture based model.
(2).	CPU is connected to Data Memory (RAM) and program memory (ROM) by a single memory.	Data Memory (RAM) and program memory (ROM) are used separately.
(3).	Common bus is used for data and program.	Separate bus is used for data and program.
(4).	used in small Computers.	used in Micro Controllers
(5).	CPU cannot access data and program at same time	Can access at the same time.
(6).	Execution speed is slower.	faster execution speed.
(7).	uses CISC	uses RISC

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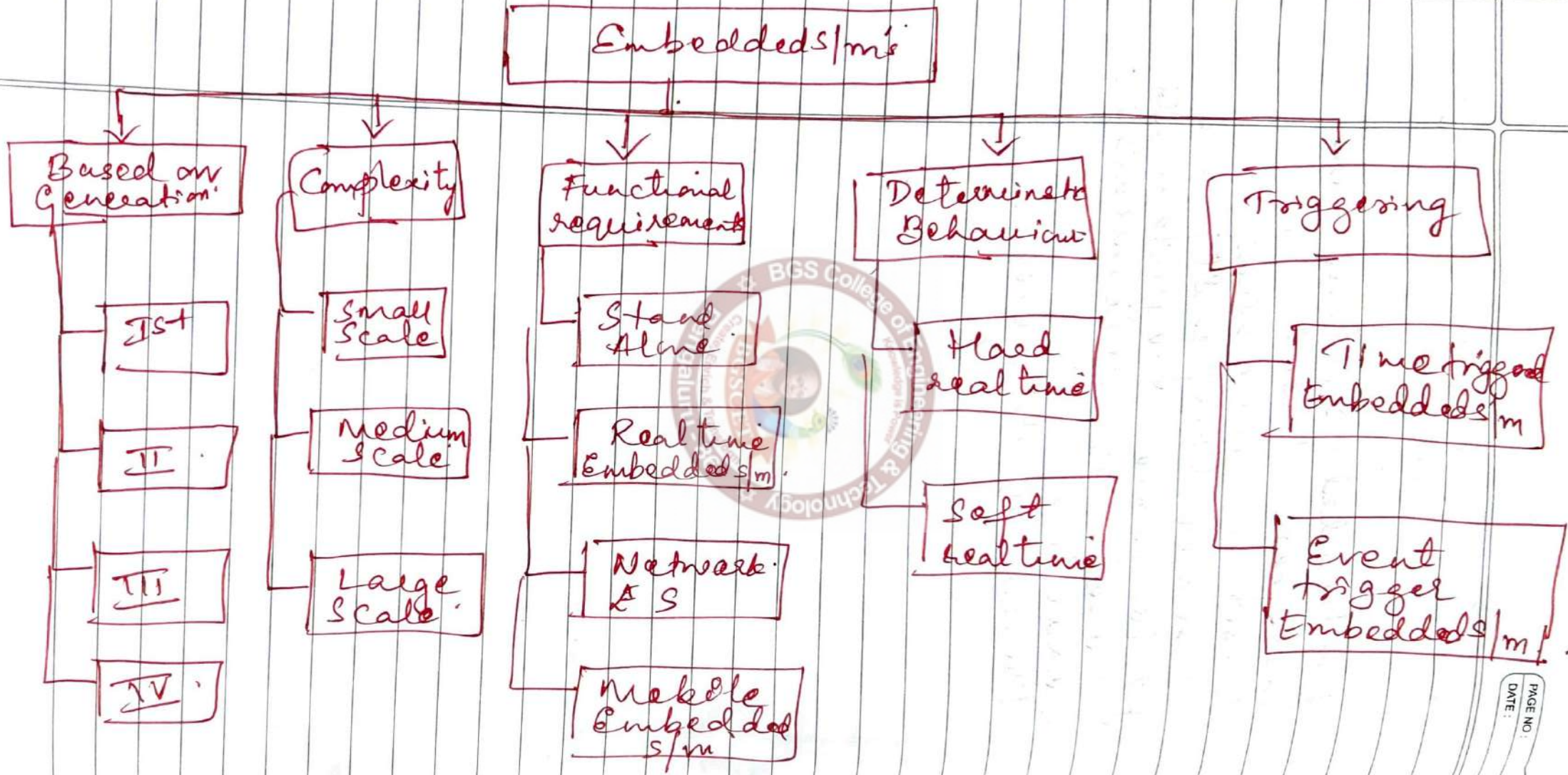
Classification of Embedded Systems :-

Embedded Systems are classified based on

- Based on Generation
- Based on Complexity and performance requirements
- Based on deterministic behaviour
- Based on triggering.


Embedded s/ms
Based on Generation
I st
II
III
IV
Complexity
Small Scale
Medium Scale
Large Scale
Functional requirements
Stand Alone
Real time Embedded s/m
Network A S
Mobile Embedded s/m
Deterministic Behaviour
Hard real time
Soft real time
Triggering
Time triggered Embedded s/m
Event trigger Embedded s/m

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→ Based on Generation :

→ First Generation :

The earlier first generation embedded systems were built with 8-bit microprocessors & 4-bit Micro Controllers.
Ex: Digital telephone keypads, Stepper motor control units.

→ Second Generation :

In this generation 8-bit microprocessors replaced by 16-bit microprocessors & 4-bit Micro controllers replaced by 8-bit micro controllers.
Ex: Data Acquisition Systems.

→ Third Generation :

Embedded Systems have 32-bit microprocessors and 16-bit Micro controllers.
Ex: Robotics, Industrial process Control.

→ Fourth Generation :

Embedded systems have high performance processors.

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→ Based On Complexity and performance Requirements:-

→ Small Scale Embedded Systems:

They are built with 8 or 16-bit microprocessor / Micro Controller.
The hardware and software Complexities are low.
Ex: Electronic toy.

→ Medium Scale Embedded System:

They are built with 16 bit or 32-bit microprocessor / micro controller.
They use programming tools like C, C++, JAVA.

→ Large Scale Embedded System:

They are built with 32bit or 64-bit microprocessor / micro Controller.
They are built with RISC processors, System on chip (SOC).

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→ Elements of Embedded System :-

Hardware

- Processor
- Power Supply
- Timers
- Counters
- I/P, O/P devices.
- Memory
- Communication Interface.

Software

- Emulator
- Compiler
- Debugger
- Assembler.

→ Major Application Areas of Embedded System :-

→ Consumer Electronics: Digital cameras, Laptops etc.

→ House hold Appliances: TV, DVD players, Washing machines, Fridges, Microoven etc.

→ Home automation & Security s/m:- AC's, Fire Alarms, Intruder detection Alarms,

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→ Automotive Industry :- Anti lock braking system, Engine control

→ Telecom :- Telephones, telephone switches.

→ Computer peripherals :- printers, Scanners, fax machines.

→ Computer Networking &/w :- Network Routers, switches etc

→ Health care :- X-ray, Scanners ECG EEG BP monitor, pulse monitor etc.

→ Measurement & Instrumentation Digital multimeters, CRO's etc

→ Banking & Retail :- ATM, Currency counters.

→ Card Readers :- Barcode, Smart Card reader etc.

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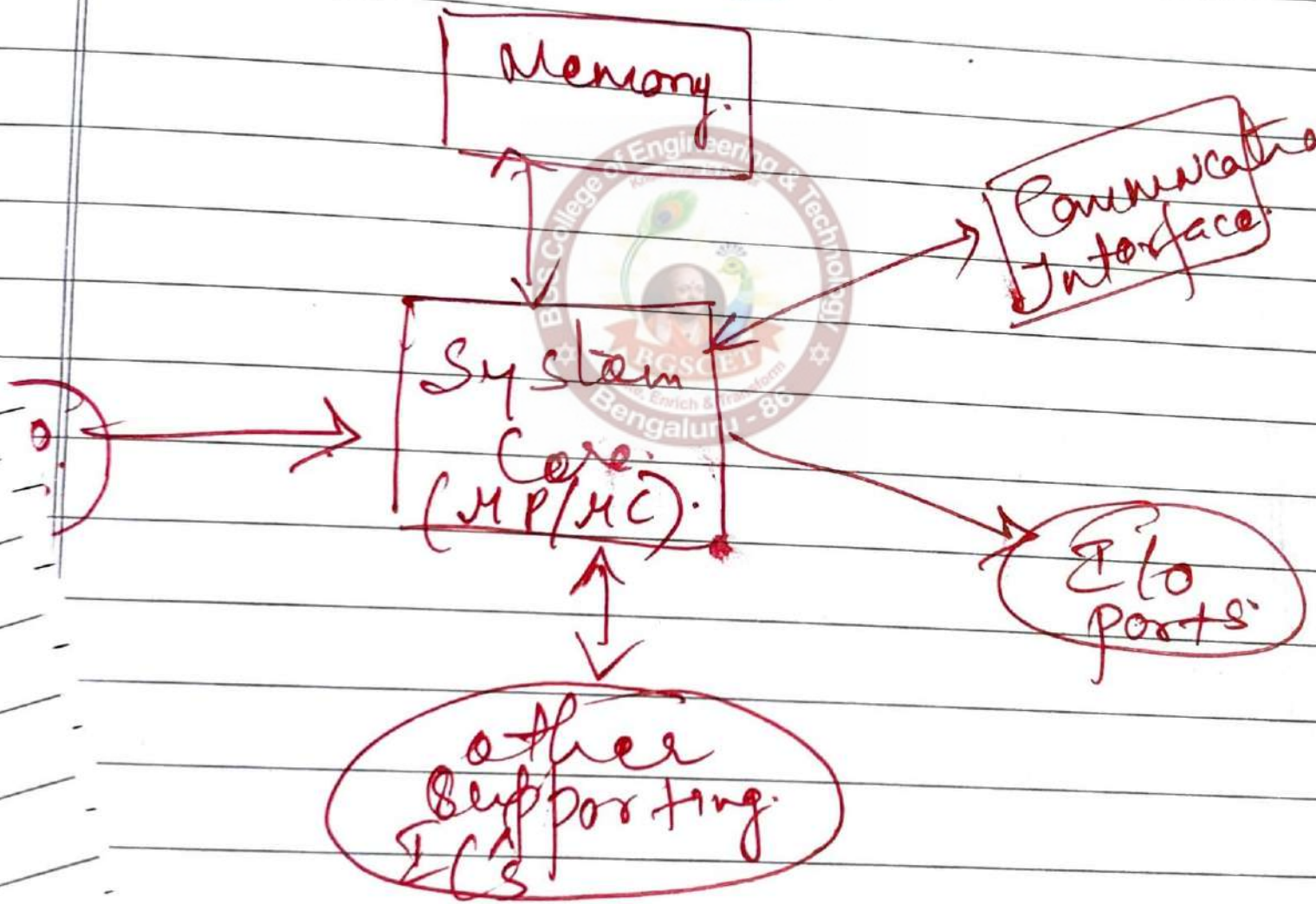
Block diagram of core of Embedded S/m.



→ The Core of the Embedded System :-

The core of the Embedded System fall in to any one of the following categories.

→ General purpose and Domain Specific processors.
  → Microprocessors
  → Microcontrollers
  → Digital Signal processors.

→ Programmable Logic Devices

→ Application Specific Integrated Circuits (ASICs).

→ Commercial off the shelf Components.

→ Sensors and Interfacing :-

Instrumentation :- Technology of measurement.

An Instrument is a device that measures or manipulates process physical variables such as temperature level or pressure etc.

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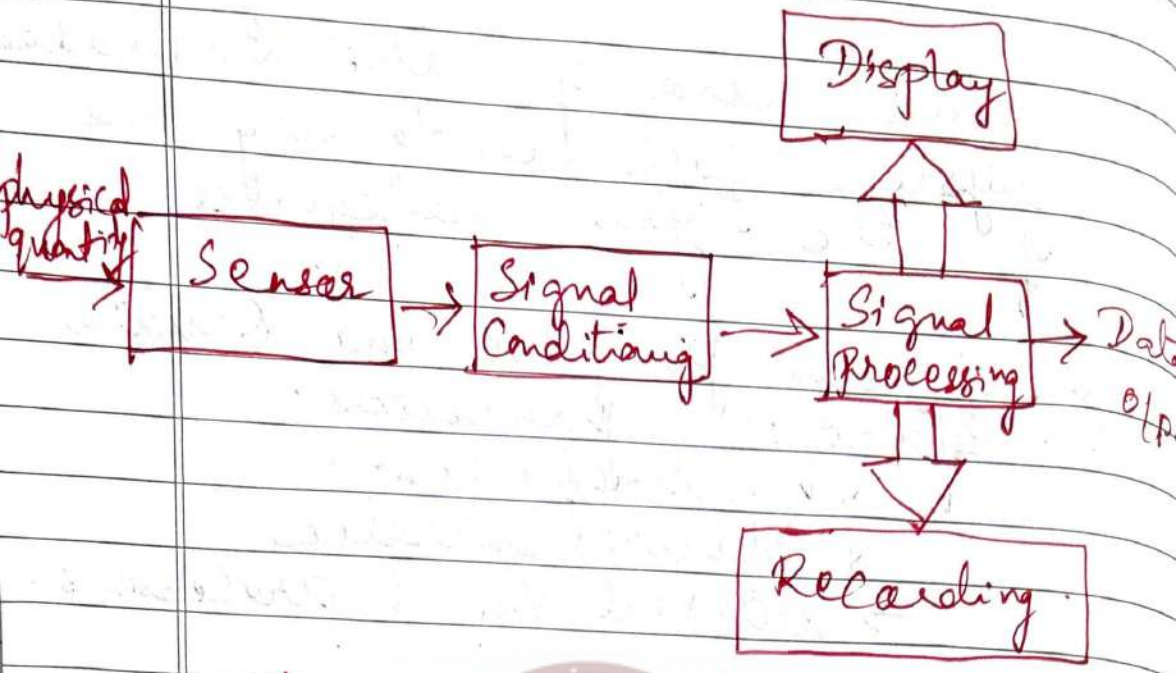
Instrumentation System :



Elements of Instrumentation Sys :

The primary element is Sensor.

⇒ The quantity to be measured is the input to the Sensor.

→ Transducer :- The sensor has non-electric input it is converted to electrical signal by means of device called transducer.

→ Signal Conditioner :- This device converts the o/p of transducer into a quantity suitable for next block.
ex: Rectification Modulation.
The electrical signal obtained from the above

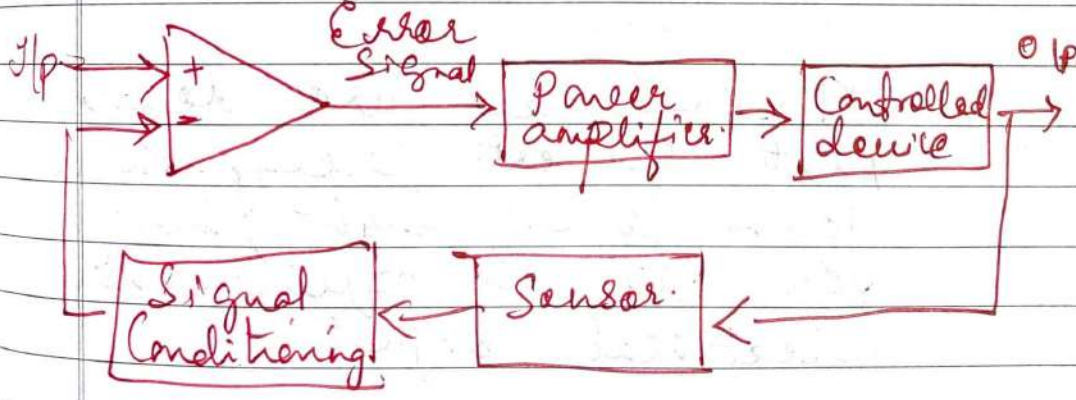
needs further conversion. If the next stage accepts only in digital form, then Analog to digital Converter is used (ADC).

→ Signal Processing Element :-

The common signal processing element is electronic amplifier. It enhances the strength of the signal. It amplifies the signal.

→ Control System :-

Control System is defined as a system of devices that manages, commands, directs or regulates the behaviour of other devices to achieve desired results.



Closed Loop Control System.

Closed loop control s/m uses -ve feedback.

I/p is given to comparator. Another I/p to comparator is O/p fed back as I/p.

If the I/p and feedback signal do not match error signal is generated.

Comparator is used to sense the difference in these two signals.

The error signal is amplified using power amplifier.

This signal is given to controller & O/p is obtained. This O/p is fed back as I/p

This signal is given to the signal conditioning block before giving as O/p.

→ Transducers :-

Transducers are devices that convert energy in the form (sound, light, heat etc) in to an equivalent electrical signal.

Energy of one form → [Transducer] → Energy of other form.

Transducer Type:

Sensor: (physical form) → (Electrical form).

Actuator: (Electrical form) → (physical form).

Ex: A microphone is a transducer converting sound pressure variations in to voltage and current.

A loud speaker is a transducer that converts low freq electric current in to audible sounds.

Sensor:-

A sensor is a transducer which converts energy in physical form to electrical energy. Sensor act as i/p device.

Ex1: Physical quantity: Sound.
I/p Transducer: Microphone
In a microphone, movement of diaphragm causes current induced in a coil.

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Sensor types:-

Sensors are 4 types.

→ Active Sensor: Generates current or voltage as output

→ Passive Sensors: This requires current or voltage as i/p.

→ Digital Sensors: O/p exist in two states ON or OFF. Low or HIGH.

→ Analog Sensors:- O/p is continuously varying.

Sensor Ex:- 2.

Physical quantity: Temperature
I/p Transducer: Thermocouple

Thermometer - measures temperature. Consists of two wires of different metals joined at each end.
One junction is placed where temp to be measured and other kept at constant

temp. This temp difference causes development of electro motive force.

Actuators:

Actuator is a transducer that converts electrical signal to corresponding physical action. Actuator acts as o/p device.

Ex:- Physical Quantity : Sound.
o/p Transducer : Loud Speaker

Light Emitting Diode (LED)

LED is an output device for visual indication in embedded s/m.

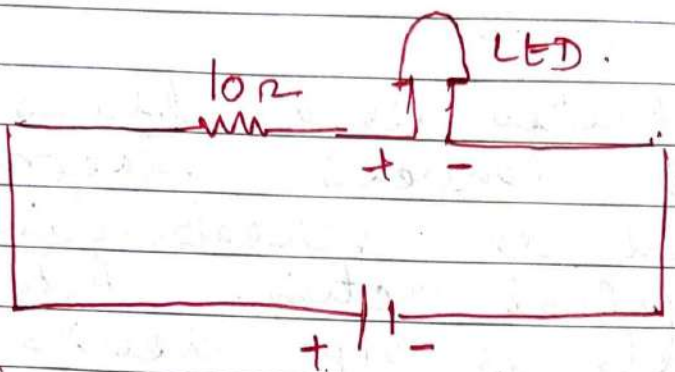
It is used as an indicator of status of various signals or situations.

Ex: Conditions like device ON/OFF

LED is a pn junction diode contains anode (+) and cathode (-).

For proper functioning anode is connected to +ve terminal and cathode to -ve terminal of supply voltage.

A resistor is used in series between the power supply & diode to limit the current through it.



Symbol for LED:

→ Interfacing LED to an Microcontroller (MC)

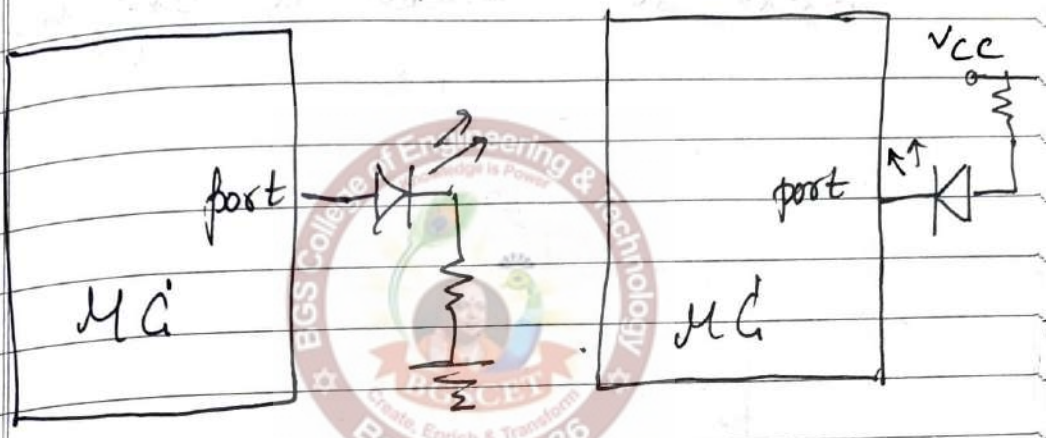
LED can be interfaced to port pin of MC in two methods.

Method 1: Anode of LED is connected to port pin. & cathode is grounded. When port pin of MP goes 1, LED is forward biased and emits light. When port pin goes 0, LED is off.

This means port pin sources current to LED. (current sourcing)

Method 2: (current Sinking)

Cathode is connected to port pin and anode is connected to supply voltage. when port pin is 0, LED turns ON.



Method - I
Current Source

Method II
Current Sinking.

→ 7-Segment LED display:-

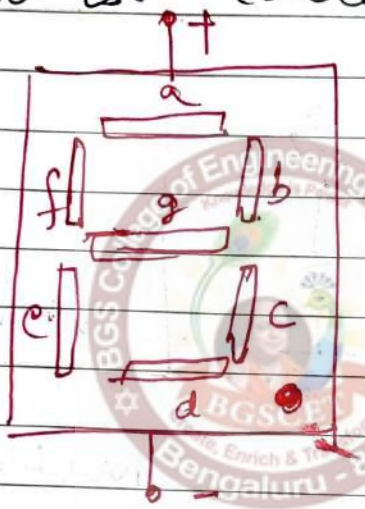
The 7-Segment LED display is an o/p device for displaying alpha numeric (0-9) and (A-F) characters.

It contains eight LED Segments arranged in a special form. 7 segments are used for displaying alpha numeric characters.

The LED segments are named A to g. & decimal point LED segment by DP.

The 7-segment LED display have two configuration
Common Anode
Common Cathode.

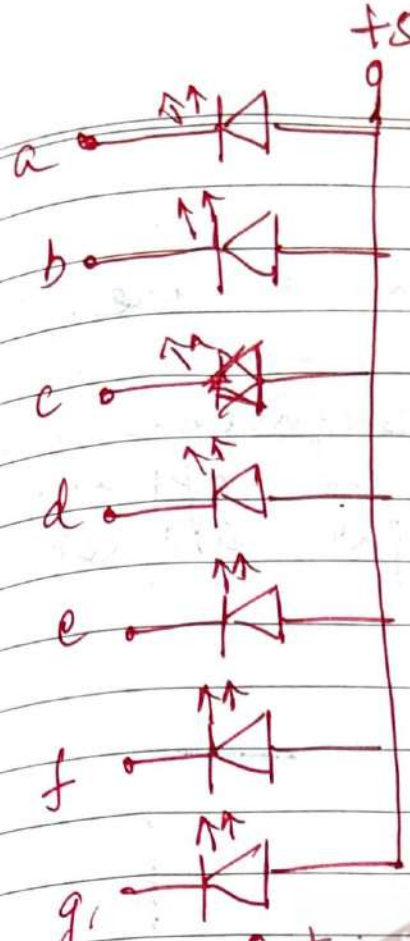
7-segment display contains 7 LED's arranged in rectangular fashion. Each LED is called a segment.

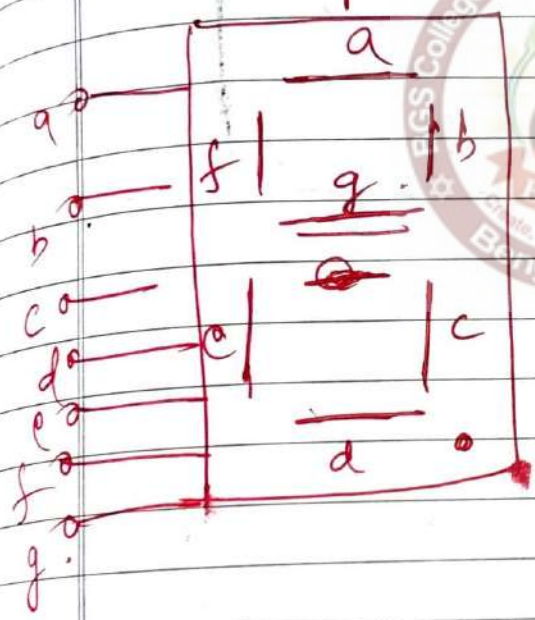


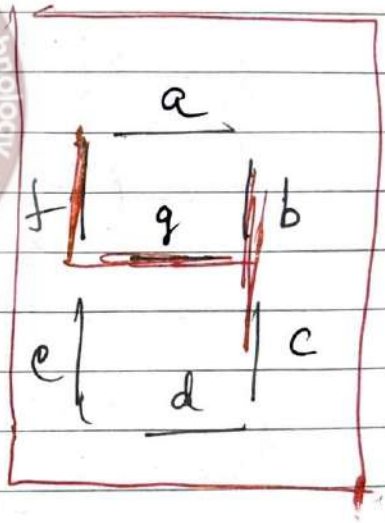
→ Common Anode Configuration

In this all anode connection of LED segments are joined together to logic 1.

The individual segments are illuminated by applying logic 0 or low signal.







Ex: To display 4. b c g f should be illuminated.
So diode b c g f to be given logic 0 to illuminate the LED's to display 4.

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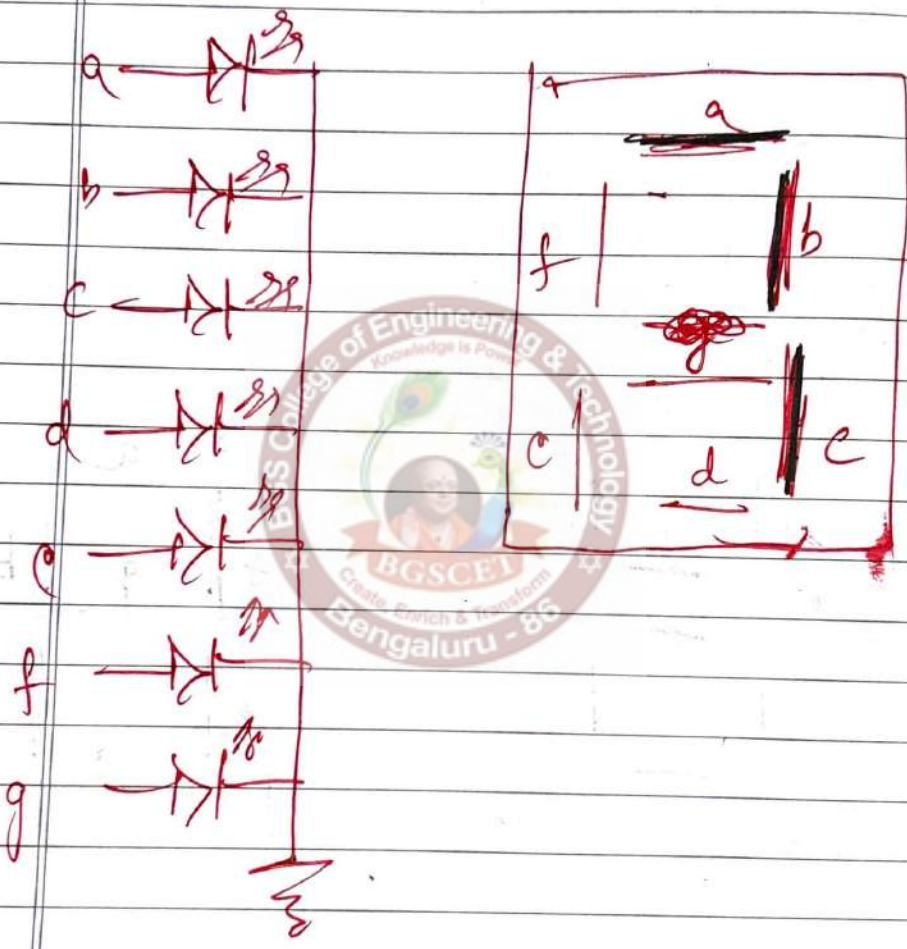
→ Common Cathode Configuration :

All the cathode are joined together to logic 0.
Individual segments are illuminated by applying Logic 1 or High signal.



Ex: for decimal number 7 to be displayed LEDs a, b, c to be illuminated So, provide logic high to a, b, and c.

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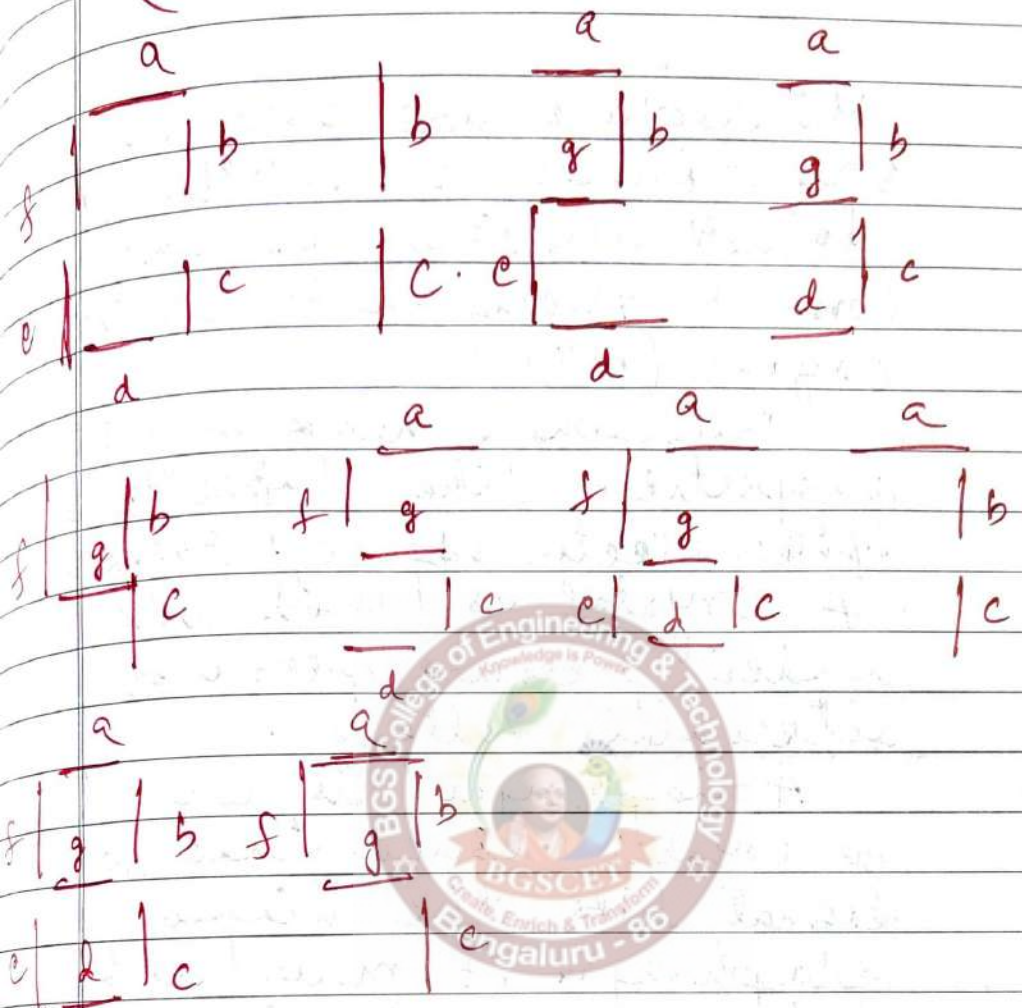
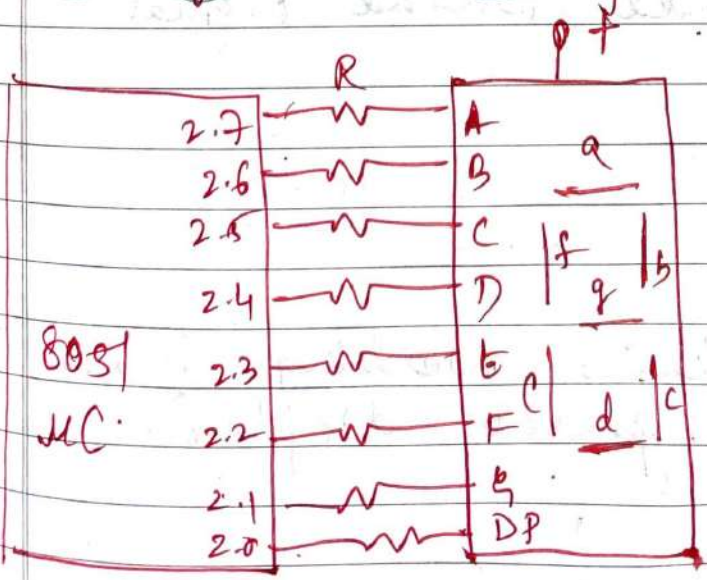
→ LED Display of ~~All~~ Numbers (0 - to 9) :-



7- LED segment Interfaced with MC:-



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→ Ex of Sensor with its operation
Explain any sensor working and operation -

Microphone are used in smart phones or mobiles. They detect audio signals and convert them in to electrical signal (mV).

Microphone work on diff properties like capacitance, piezo electric effect, resistance. A crystal is used which under pressure produces alternating voltage.

A diaphragm is connected to crystal such that sound signal hits the diagram diaphragm it moves to & fro, that causes vibrations in crystal & produces alternating voltage generated for the applied sound signal.

→ Explain any Actuator working principle.

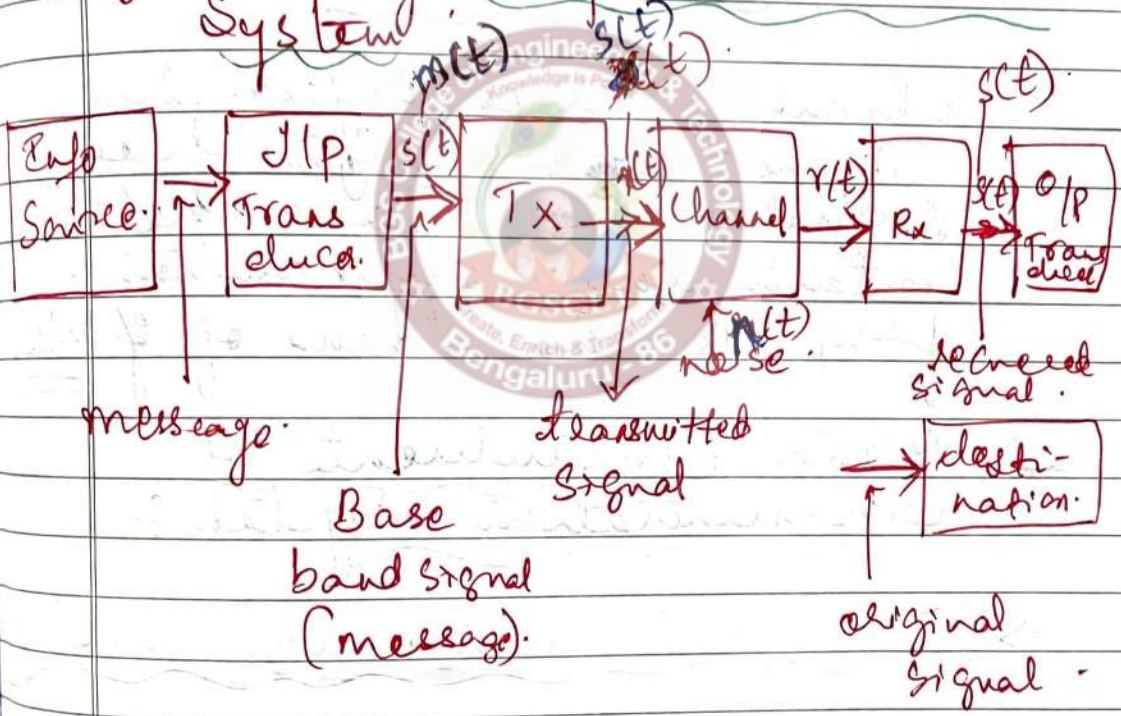
Explain working of LED - 7 segment display.

Module 5. Analog And Digital Communication:

Modern Communication System:

→ Communication engg deals with transmitting information
→ Information is transmitted through electrical signals.
→ Information is transmitted through Communication link.

Block diagram of Communication System:



The main constituents of Communication System are:

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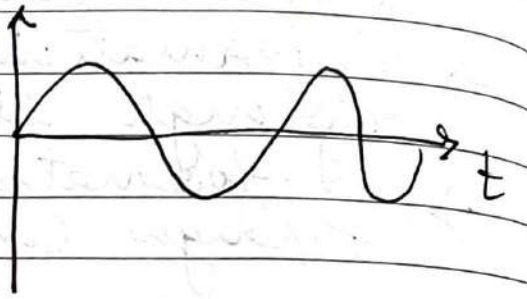
Note ① Message Signal :- The signal that contains information is called message signal. It is a low freq signal. (20 Hz - 20 kHz)



Note ② : Carrier Signal : The signal carries information signal. It is high freq signal and does not contain any information. freq is in terms of MHz.

→ Main constituents of communication system :-

→ Information Source and Transducer

Message or information originates in the information source may be in form of sound (human speech) picture (image) words (text)

A transducer is a device which converts one form of energy to other.

I/p transducer (Sensor)

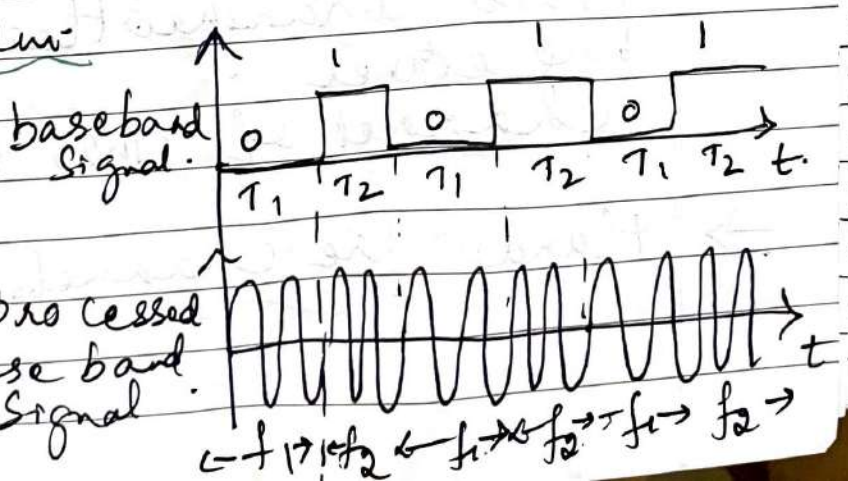
Converts sound/light signal to electrical signal.

→ Transmitter :-

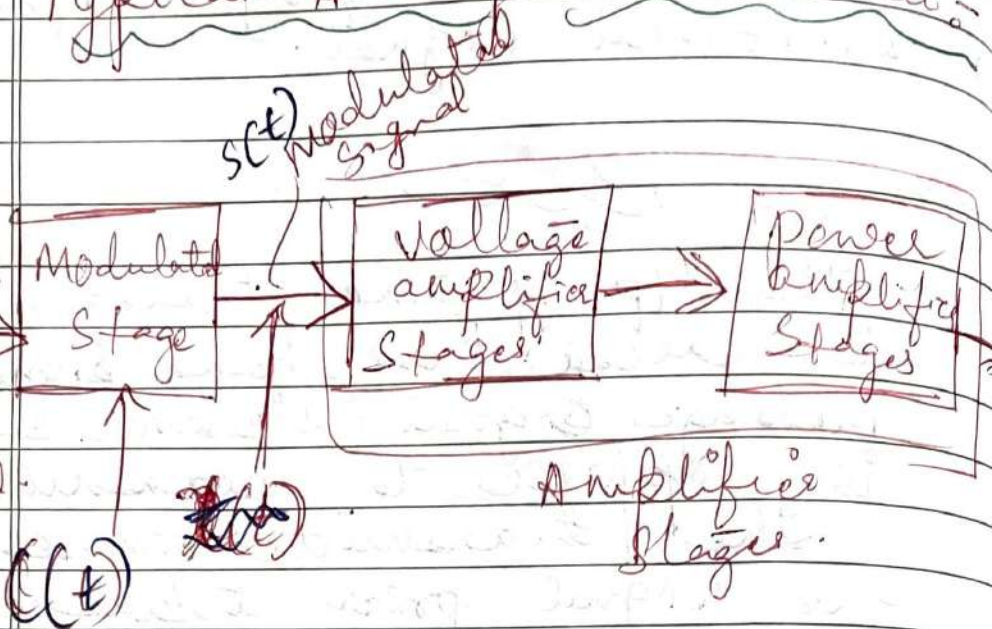
The O/p of the transducer is called base band signal/ message signal (electrical signal) is applied to transmitter.
The transmitter processes the signal prior transmission

→ The baseband signal is low freq signal. It is translated to high freq called Carrier Communication System
In this system main function of transmitter is Modulation. In modulation message signal is superimposed on higher freq signal.

→ The baseband signal is transmitted without translating into high freq. is called Baseband Communication System



→ Typical Analog Transmitter:-



m(t) be the base band signal. It is given to modulator. and converted to high freq signal. The modulated signal is s(t). This signal is amplified using amplifier stages. The amplified signal is passed to the channel.

→ Channel / Medium:-

The medium through which message travels from transmitter to receiver.

Channel of two types:

→ Hardwire channels (Manmade structures):-

→ Transmission Lines:

Consists of two or more conductors through which signals are transmitted

ex: ① Twisted pair cables used in telephony.

② Coaxial cables. used in TV transmission.

→ Wave guides:-

Consists of hollow metal tube for transmitting signals

→ Optical fibre:-

Consists of very thin hollow glass fibre through which signal is transmitted in form of light energy.

→ Softwired channels (no physical connection b/w Tx and Rx)

Natural resources used as medium for transmission

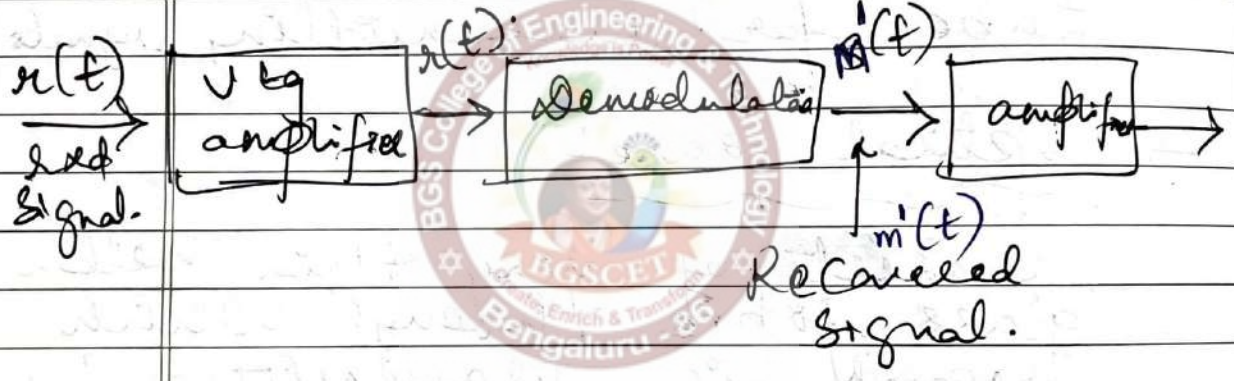
ex: air / open space
sea water.

→ Noise: noise is defined

as unwanted Signal. It is undesirable part of Communication System. When noise is mixed with signal it gets deteriorated.

→ Receiver:

The function of receiver is to reproduce original signal. This is done by process called demodulation or detection.



The signal received is r(t) It is a weak signal as noise is present in the signal. It is amplified. Then given to demodulator. Here base band signal is separated from modulated signal. The original base band signal is m'(t) This is given to destination.

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→ Destination :- Here message signal is converted in to original form using o/p transducer & then given to destination.

→ Explain noise, noise factor & noise figure & signal to noise Ratio :-

→ Noise :- This is an unwanted disturbance / signal in communication s/m.

destination

→ Signal to Noise Ratio :- (SNR)

SNR is defined as ratio of signal power (S) to noise power (N) It is expressed in decibels (dB).

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{\text{Wanted}}{\text{unwanted}}$$

$$\frac{P_S}{P_n} = \frac{S}{N}.$$

$$P_S = V_S^2/R \qquad P_n = V_n^2/R.$$

$$\frac{S}{N} = \frac{P_s}{P_n} = \frac{V_s^2/R}{V_n^2/R}$$

$$\frac{S}{N} = \frac{P_s}{P_n} = \frac{V_s^2}{V_n^2}$$

$V_s \rightarrow$ Signal voltage
$V_n \rightarrow$ noise voltage.

$$(SNR)_{dB} = 10 \log\left(\frac{V_s^2}{V_n^2}\right)$$

$$\left(\frac{S}{N}\right)_{dB} = 20 \log\left(\frac{V_s}{V_n}\right).$$

Ex:- In a circuit Signal and noise voltages are 3.5mV and 0.75mV respectively. find SNR in dB.

$$\left(\frac{S}{N}\right)_{dB} = 20 \log\left(\frac{3.5}{0.75}\right)$$

$$= 13.38 \text{ dB}.$$

→ Noise factor :- (F)

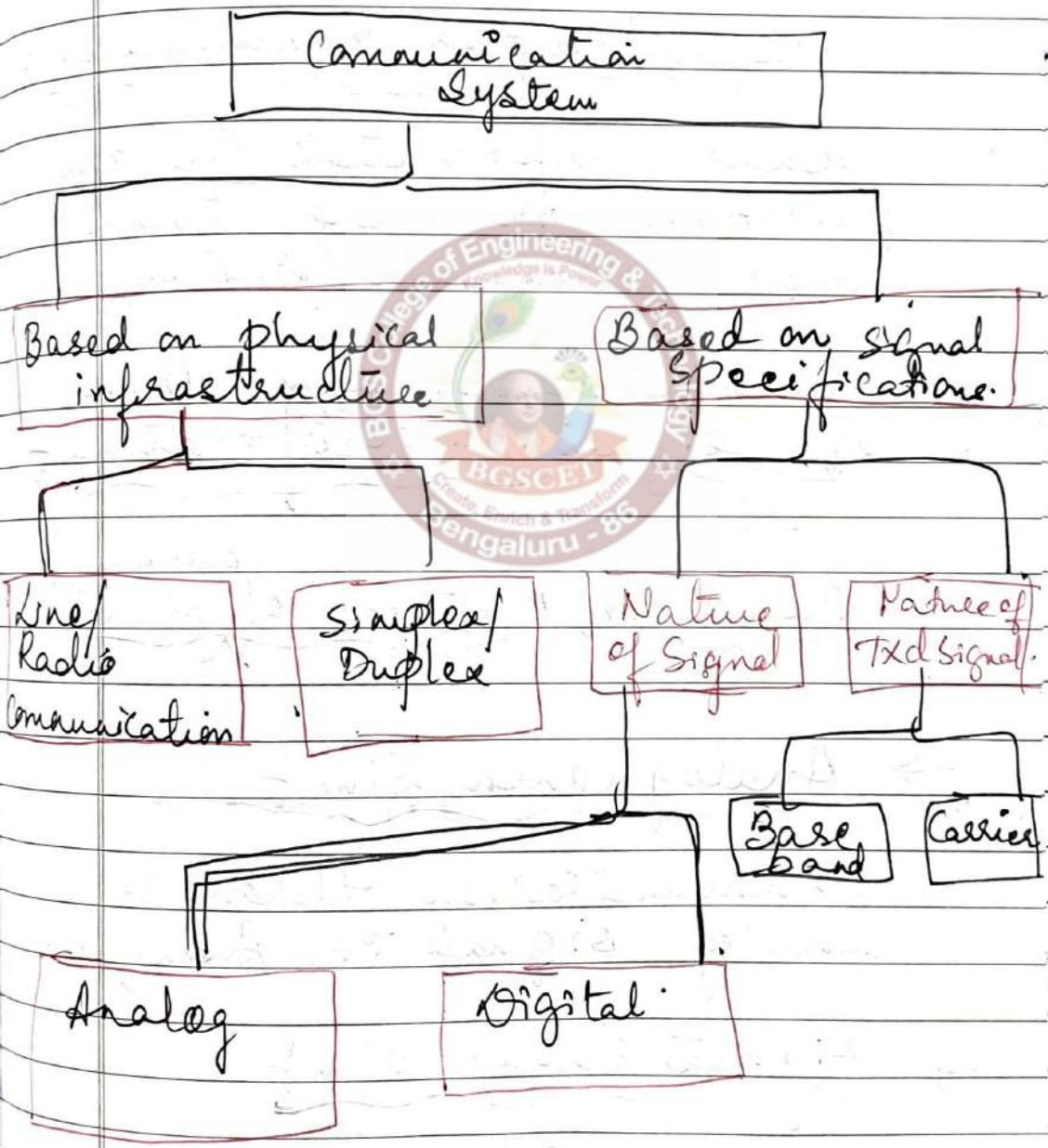
$$F = \frac{\text{SNR at i/p}}{\text{SNR at o/p}}.$$

→ Noise figure :- (NF)

$$NF = 10 \log F$$

$$NF = 10 \log \left(\frac{SNR_{ip}}{SNR_{op}} \right)$$

→ Types of Communication System



→ Communication Sfm based on physical infrastructure:-

→ Line Communication System:-

use power lines to transfer data from one point to another point

→ Simplex / Duplex Communication:-

Sends information in one (simplex) or more than one direction (duplex).

→ Communication Sfm Based on Signal Specifications:-

→ Based on nature of baseband Signal:-

→ Analog Comm Sfm:-

Communication through analog signals Ex: Audio, Video

→ Digital Comm Sfm:-

Communication through digital signals
Ex: HDTV.

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→ Based on Nature of Transmitted Signal :-

→ Base band Comm Sys :-

Base band signals transmitted without translating to higher freq's.

→ Carrier Comm Sys :-

Base Band signals are mixed with high freq signals and transmitted.

→ Multiplexing :-

Multiplexing is a process that allows more than one signal to be transmitted through a single channel. Multiplexing is done through modulation.

In multiplexing each baseband signals are modulated with diff carrier frequencies and transmitted.

At the receiver transmitted signals are separated based on their carrier freq's.

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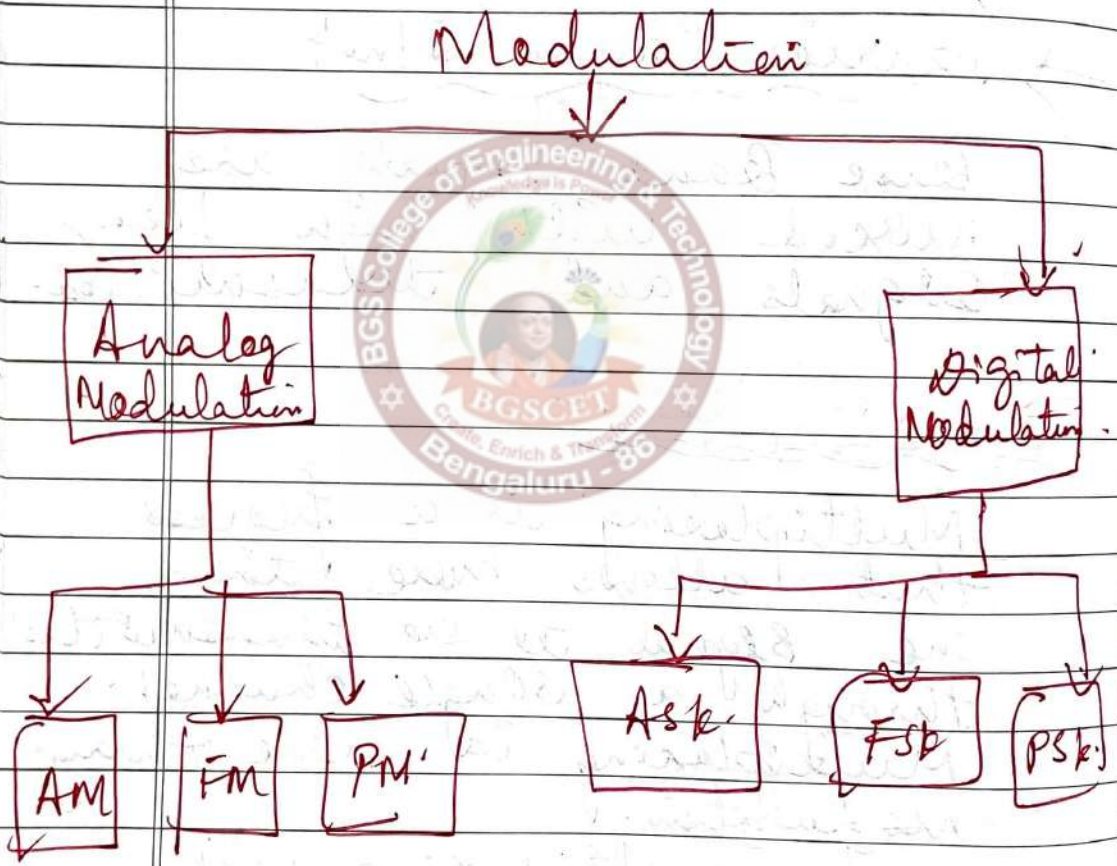
→ Modulation :-

Modulation is the process in which any one parameter (Amplitude, freq, phase) of carrier is varied in accordance with the message signal with other parameters constant.



AM - Amplitude Modulation } Analog
FM - freq modulation } Modulation
PM - phase modulation }

Ask - Amplitude Shift keying.
Fsk - freq Shift keying
PSk - phase Shift keying.

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→ List the advantages of digital communication over Analog communication.

→ Communication using digital signals are stable and less prone to noise.
→ Digital signals use discrete values to represent data.
→ Digital signals use less power.
→ Digital signals are not corrupted during data transmission.

→ Briefly describe analog modulation types in detail.

→ Amplitude Modulation : It is the process in which amplitude of the carrier signal is varied in accordance with the message signal with freq and phase constant.

The amplitude of carrier increase with increase in amplitude of m(t) and decreases with decrease in amplitude of m(t).

Digital Modulation

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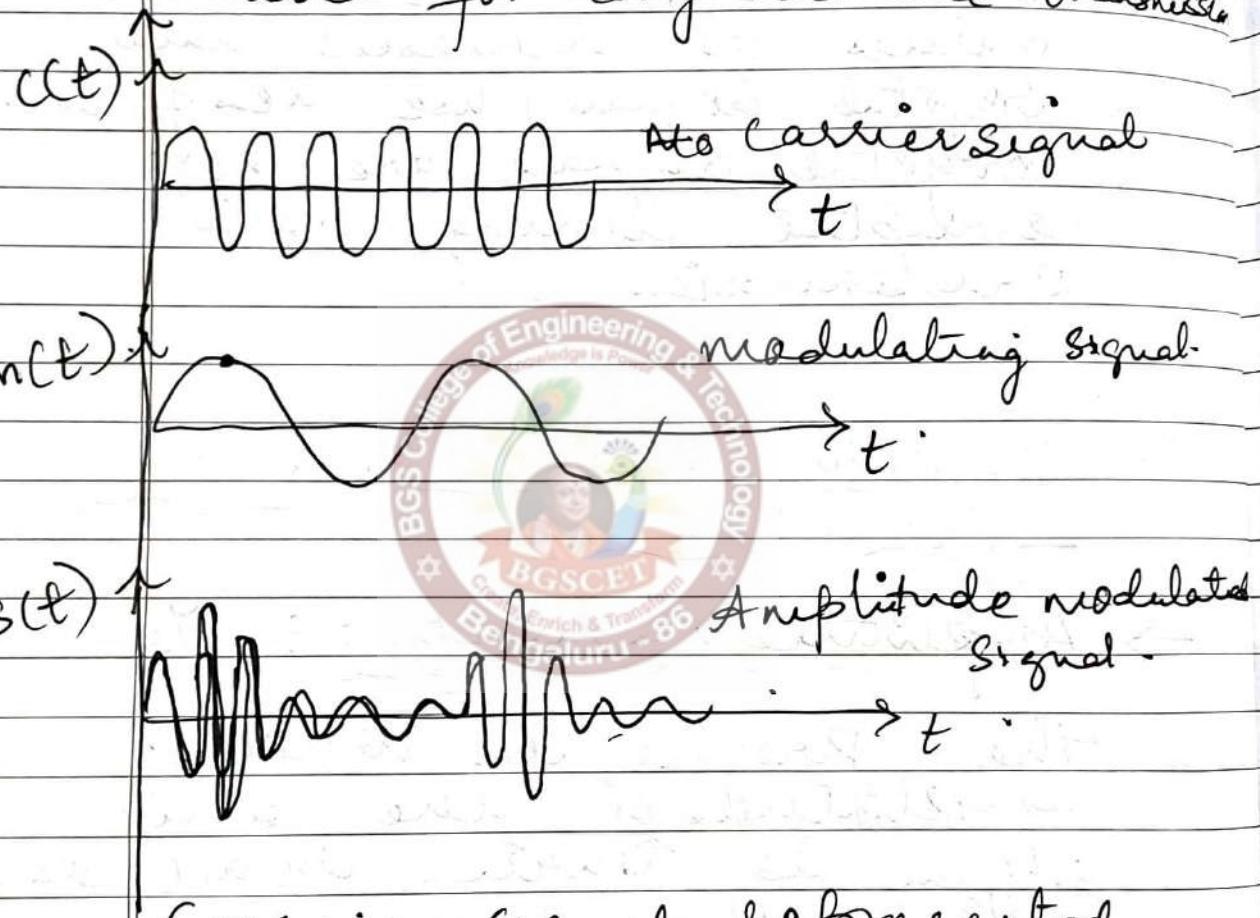
→ Amplitude Modulation : (AM)

Is the process in which amplitude of carrier signal varies with message signal. freq and phase of carrier are constant.

used for long distance transmissio



Carrier signal represented by $c(t) = A_c \cos(2\pi f_c t)$

Message signal represented by $m(t) = A_m \cos(2\pi f_m t)$.

$A_m \rightarrow$ Amplitude of $m(t)$
$A_c \rightarrow$ Amplitude of $c(t)$
$f_m \rightarrow$ freq of m(t)
$f_c \rightarrow$ freq of $c(t)$.

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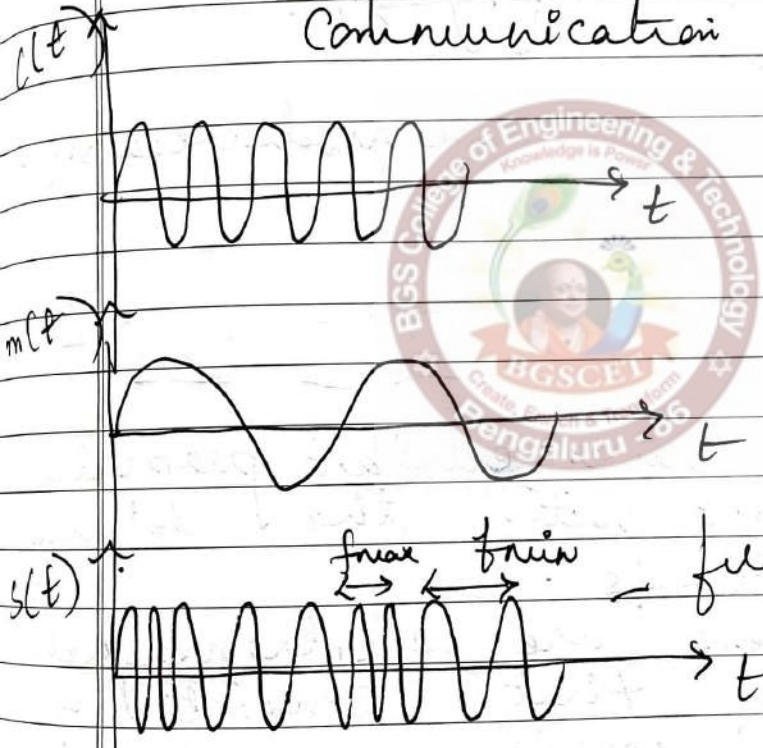
→ Frequency Modulation:-

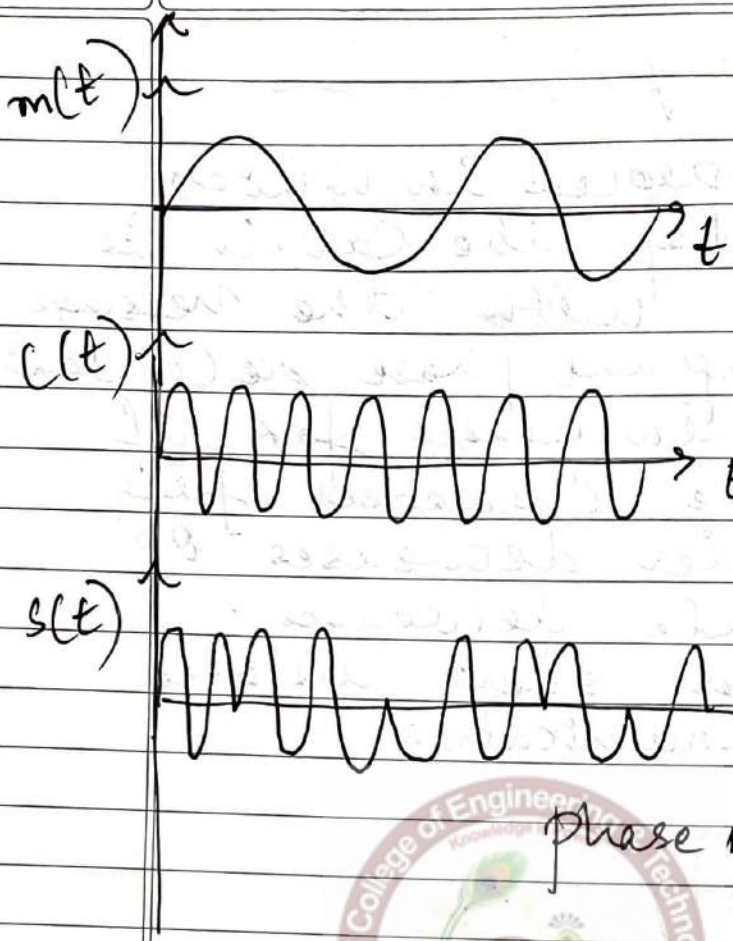
Is the process in which frequency of the carrier is varied with the message signal. Amp and phase are constant freq increases for ↑ of amplitude ↑ increases. freq of carrier decreases ↑ of amplitude decreases.
used for short distance communication.



freq modulated signal.

→ Phase Modulation:-

Phase of the carrier is varied with the message signal. Amplitude and freq are constant.



Phase modulated signal

→ Radio Wave Propagation :-

Radio waves exhibit properties of light with the velocity of 3×10^8 m/s.

These are electromagnetic waves that consists of electric fields and magnetic field components.

Radio waves travel from one end to another end.

Radio propagation is the way of transmitting radio signals in different ways.

→ Ground Wave or Surface Wave

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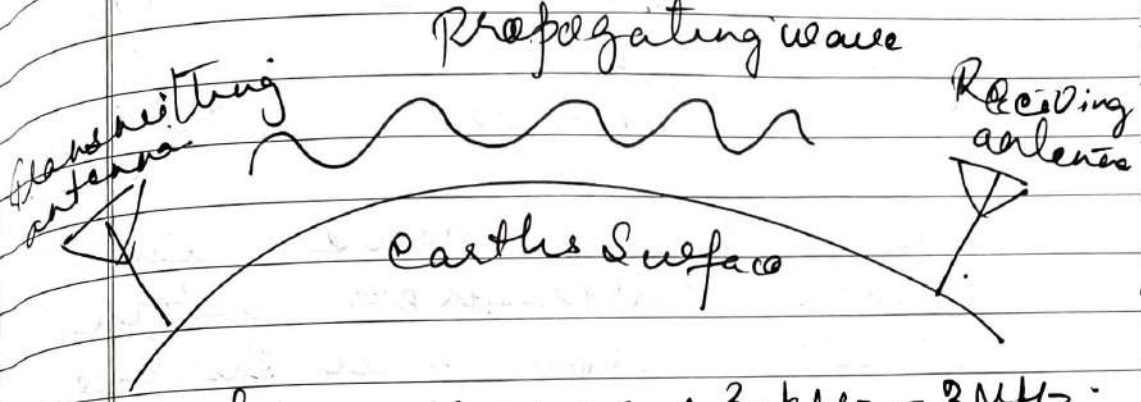
Ground wave travel from transmitting antenna to receiving antenna over the earth's surface.



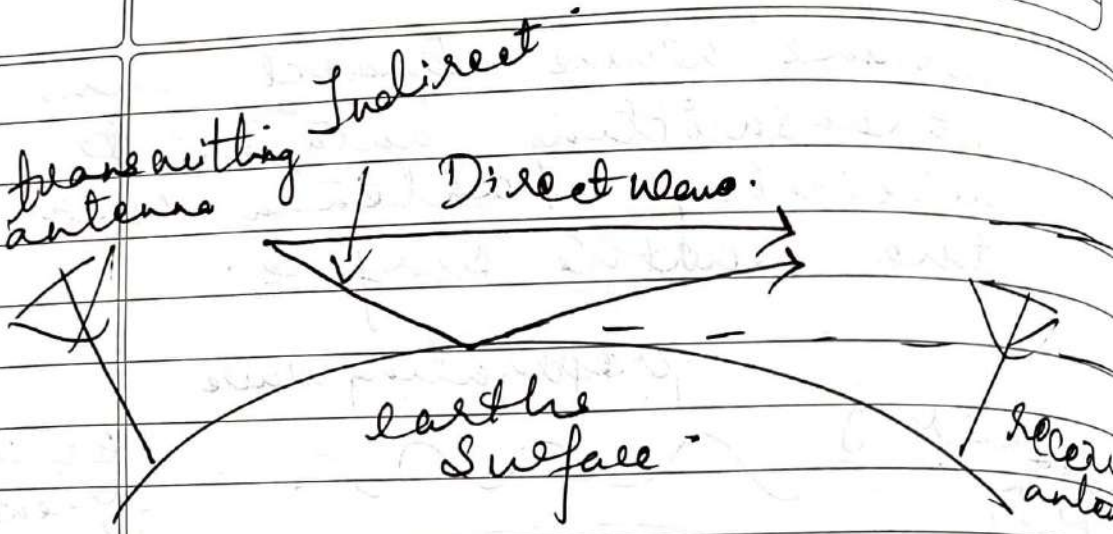
freq range : 30kHz - 3MHz.
Transmission distance : 100-1000km

→ Space or Tropospheric Wave:

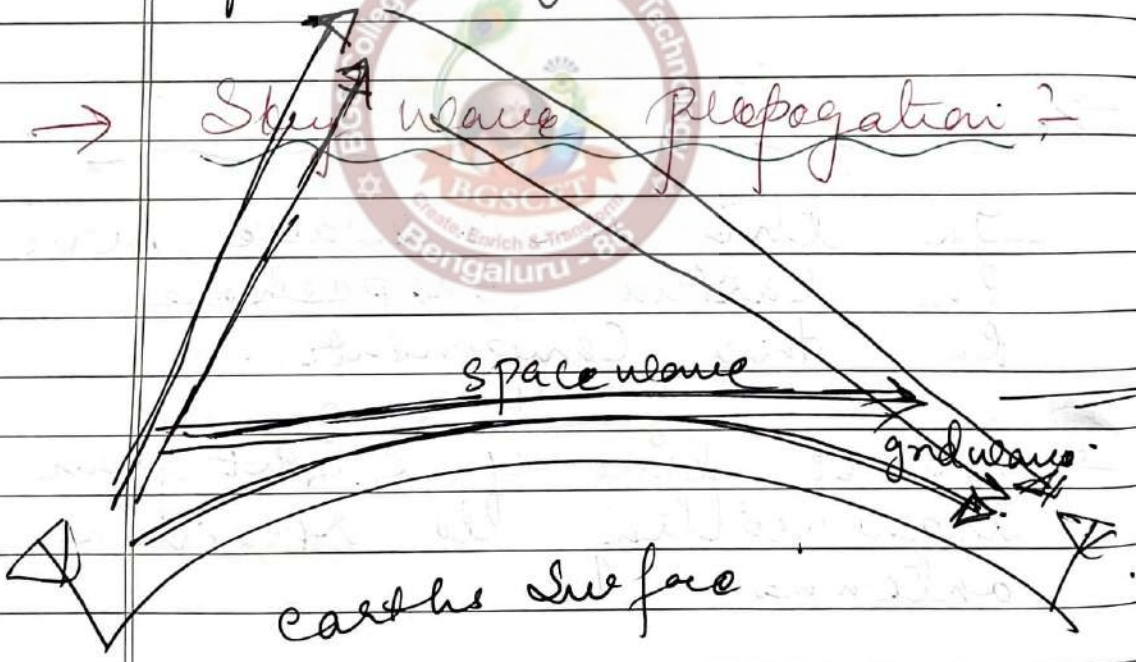
In this radio wave move on earths troposhere in two components.

→ direct line of sight from transmitting to receiving antenna

→ Indirect or ground reflected wave from transmitting antenna to ground and then to receiving antenna.



radio waves move in earth's troposphere within about 0-12km over surface of the earth.
Freq range is 3 MHz - 30 MHz



→ Sky wave propagation :-

Radio waves transmitted from transmitter reach the receiver after reflection from the ionosphere (earth's upper atmosphere).

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→ Digital Modulation Schemes:

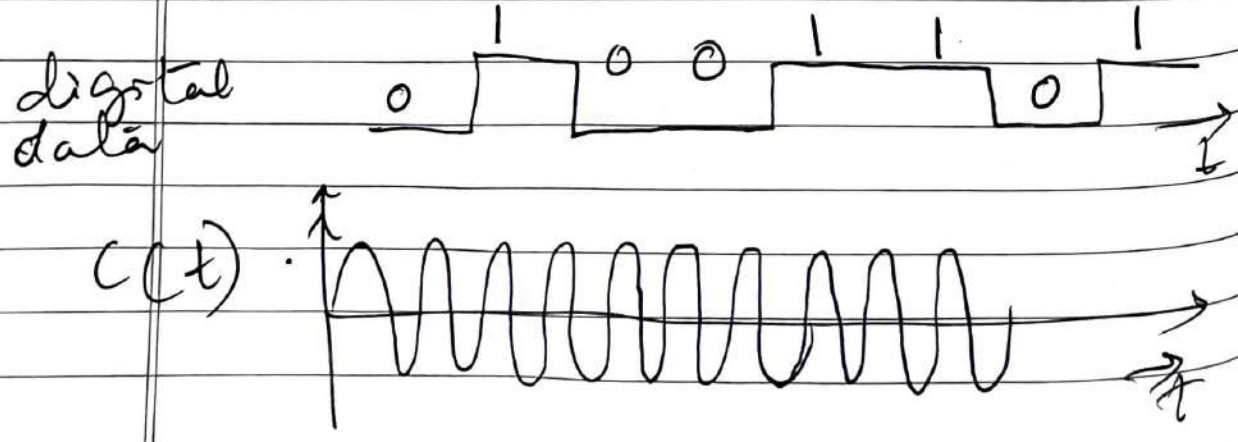
In communication if the base band signal consists of 1's and 0's (binary data) then it is called Digital Communication.

If the amplitude or freq or phase of the carrier changes with binary data then it is called Digital Modulation schemes

The Digital modulation schemes are:

Amplitude Shift keying (ASK)
Freq Shift keying (FSK)
Phase Shift keying (PSK).

→ ASK: The amplitude of the carrier exists if base band signal is 1 and amplitude of carrier is 0 if base band signal is '0'.



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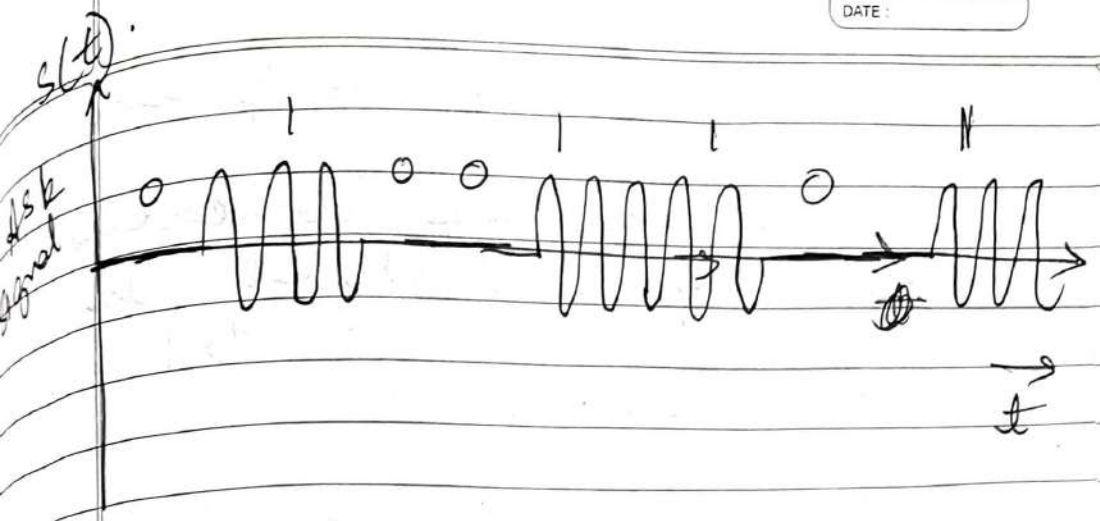
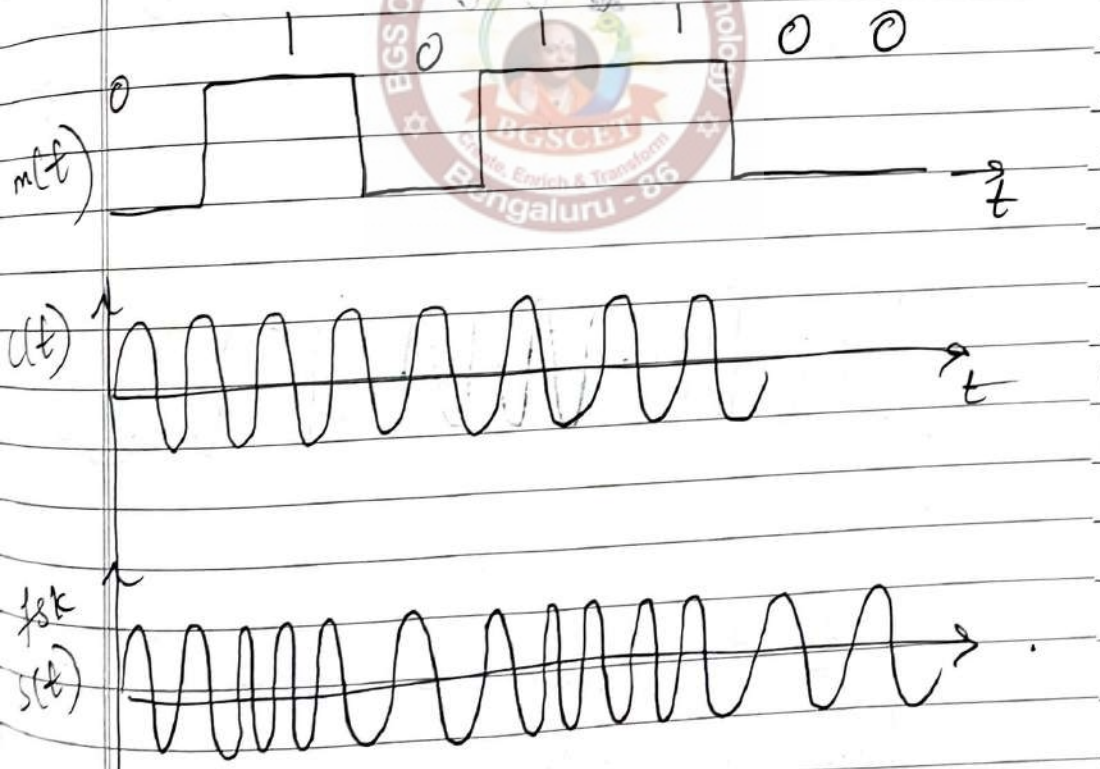
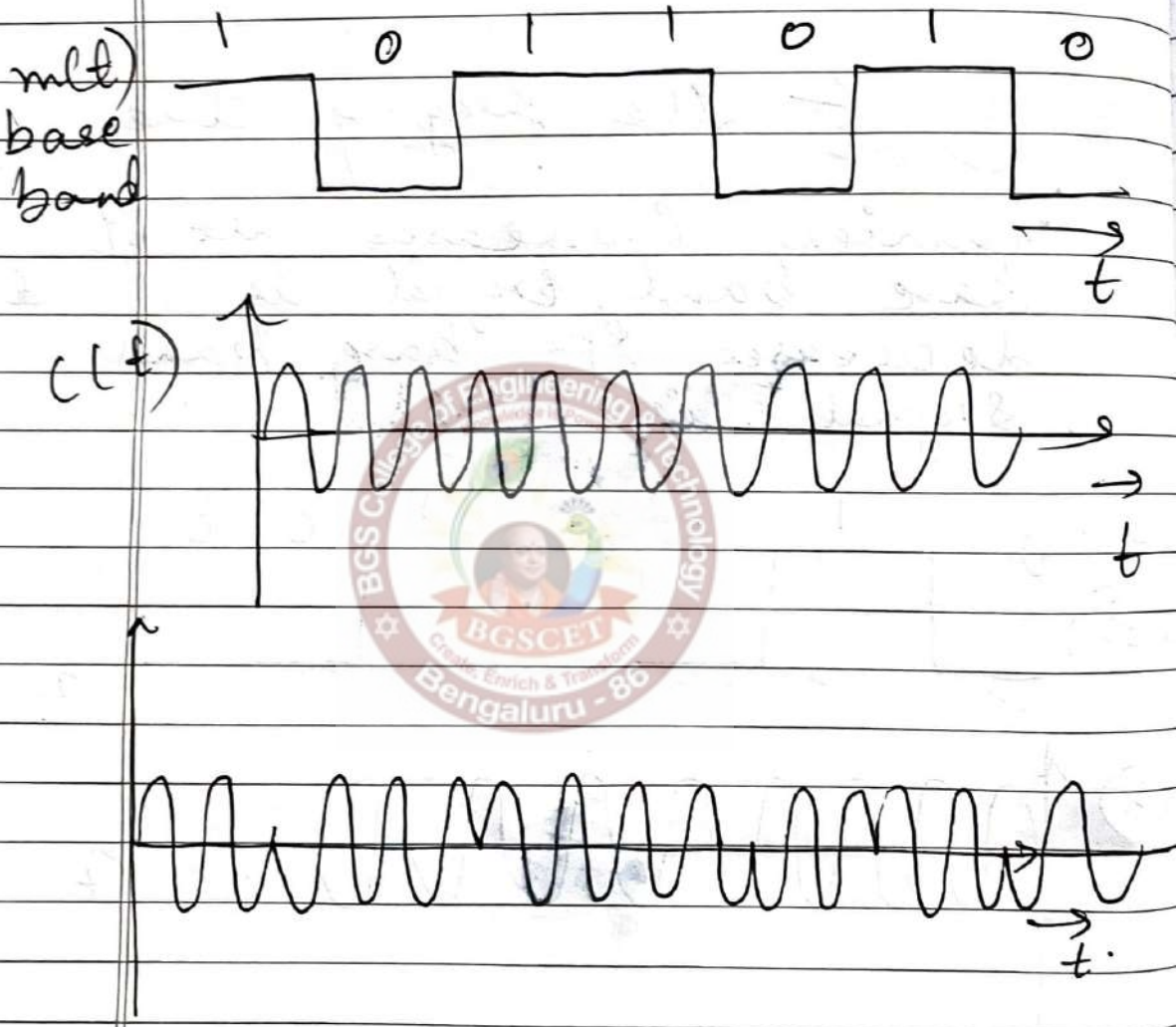


→ FSK :- The freq of the carrier increases when i/p of base band signal is '1' and decreases if/p of base band signal is '0'.



→ PSK :- The phase of the carrier changes whenever base band signal has transition from 0 to 1 and vice versa.



→ Radio Signal Transmission :-

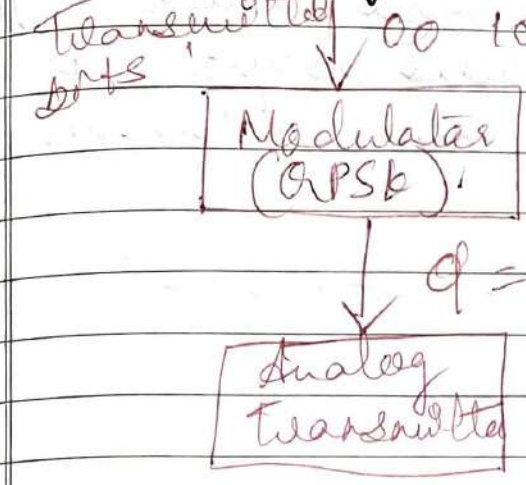
The wireless transmitter accepts four different binary stream of bits.

Transmitter operates in two stages

→ Quadrature phase Shift keying (QPSK)

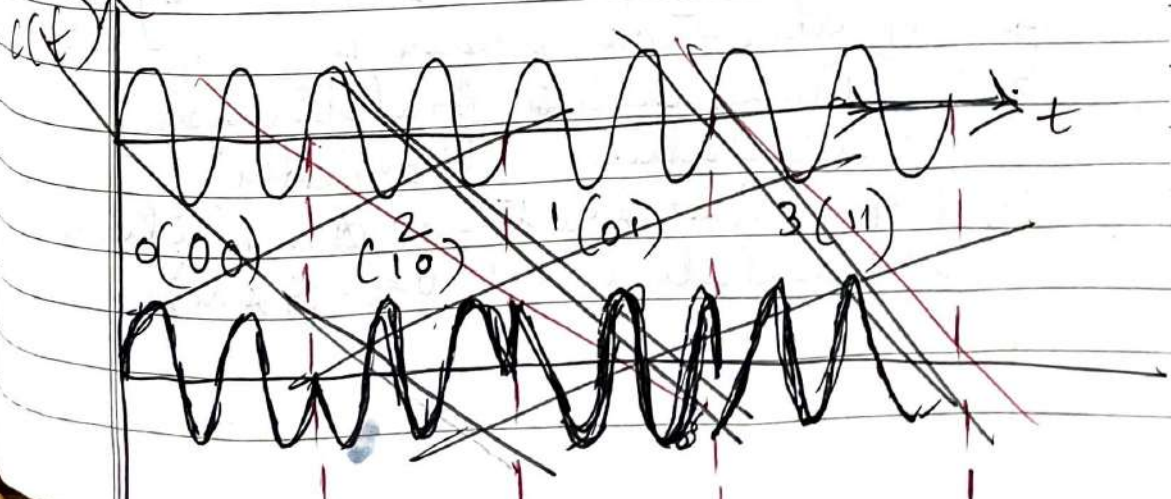
Q. QPSK TX with W/F and Constellation Diagram and Analog transmitter.

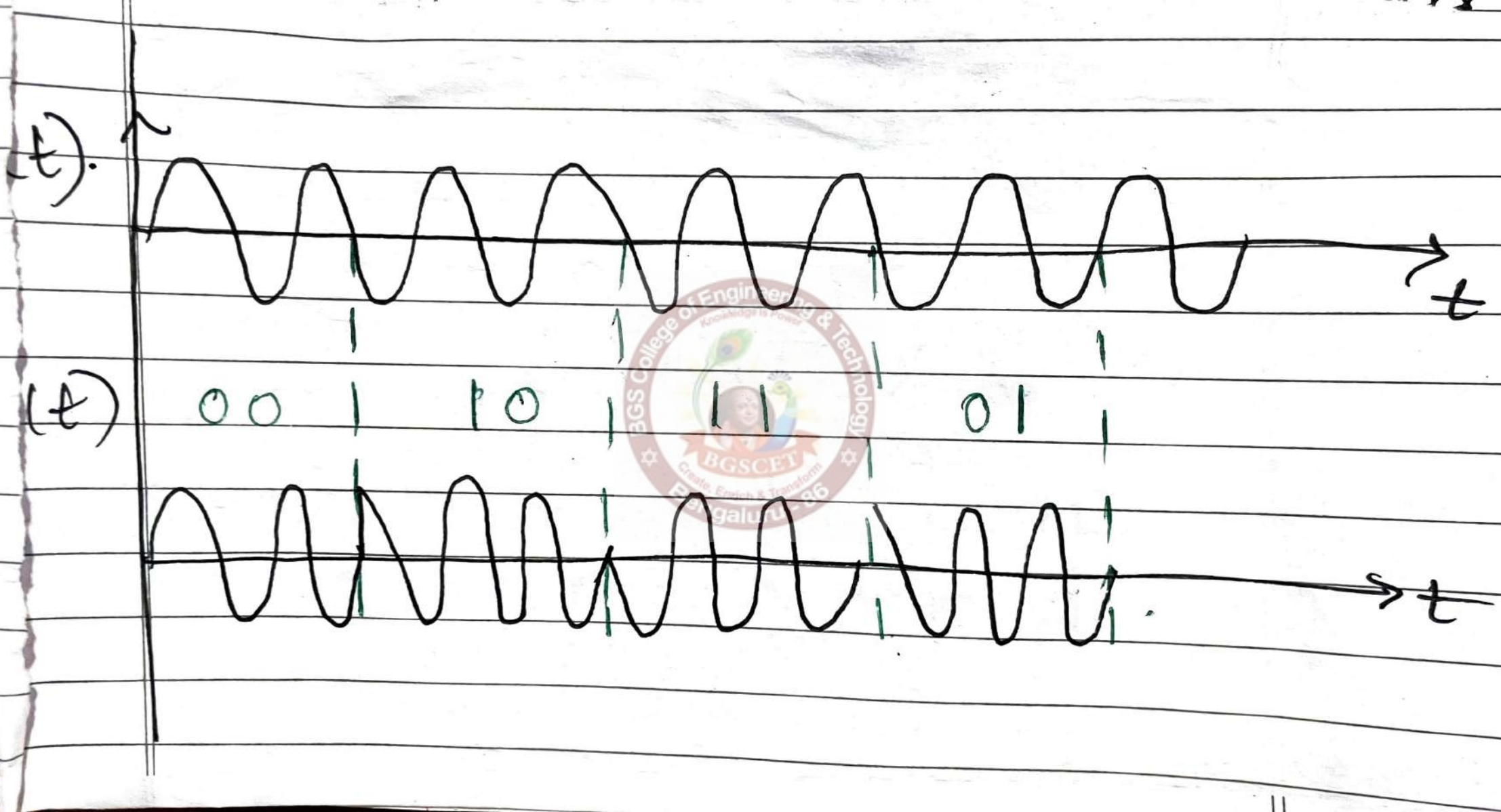
→



QPSK: Is a modulation technique in which modulator takes two bits at a time. Two symbols are modulated at a time. The carrier is varied as per the symbols with phase change.

Symbols	Phase change ϕ
00	0°
10	90°
11	180°
01	270°




(t).
t
(t)
0 0
1 0
1 1
0 1
t

The analog transmitter transmits the modulated wave. This generates radio wave is generated and transmitted.

Constellation diagrams:-

Q) Describe Radio Signal Transmission

→ Transmission Modes in Mobile Communication System

Long term Evolution (LTE) is a standard for wireless broad band communication for mobile devices marketed as 4G. LTE uses four modulation schemes.

→ Binary phase Shift Keying.
→ Quadrature phase " "
→ 16-Quadrature Amplitude modulation (16 QAM)
→ 64-Quadrature Amplitude modulation (64-QAM).

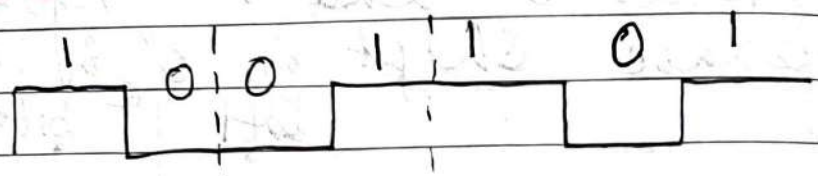
→ BPSK:- BPSK is binary shift keying uses two states 0 and 1 representing phase shift of 0° & 180°.

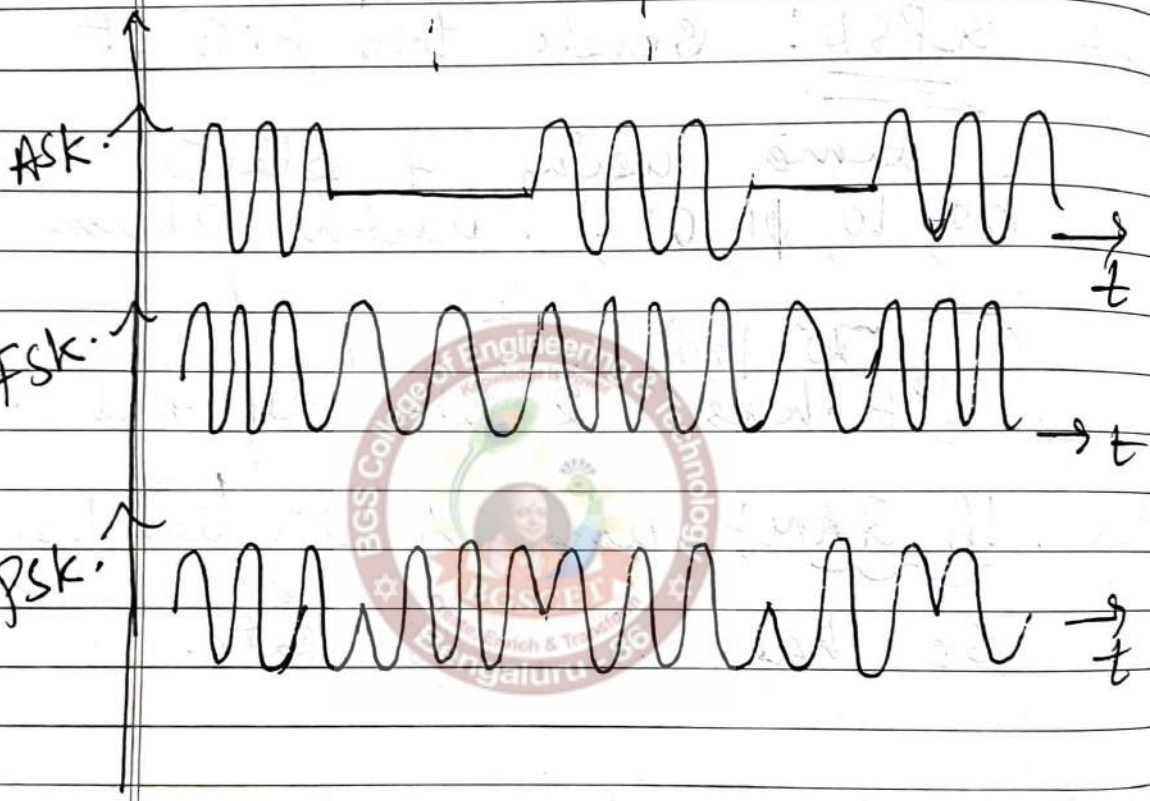
→ QPSK:- Sends two bits at a time using 4 states (00, 10, 01, 11) with phases (0°, 90°, 180°, 270°) It has 2 bits/symbol.

→ 16 QAM:- uses 4 bits/symbol so has $2^4 = 16$ states.

→ 64 QAM:- uses 6 bits/symbol so has $2^6 = 64$ states.

→ Consider full binary data & Sketch ASK, FSK and PSK.





→ Q. Describe Multiple Access Techniques.

Multiple Access technique:-

Is a technique to provide communication service to multiple users over a single channel.

It allows multiple mobile users share the alloted spectrum.

There are 3 types: (FDMA)

→ Freq division Multiplexing Access:

The available freq band is split in to smaller freq bands and assigned to users.

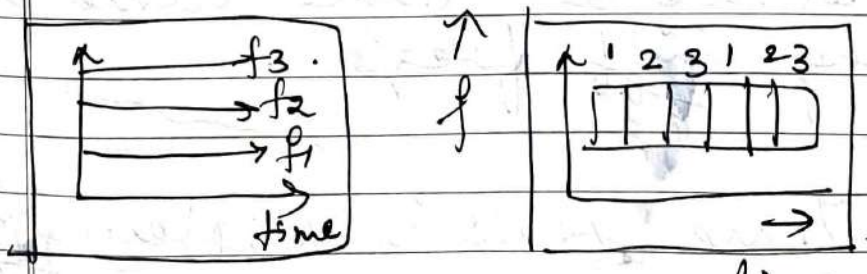
→ Time Division Multiplexing: (TDMA) Access

Various users can transmit at same freq band at different times.

→ Code division Multiple Access (CDMA)

Mobiles receive signals on the same freq and at same time. But signals are labelled by use of code.

(3G technologies are built).



FDMA TDMA.

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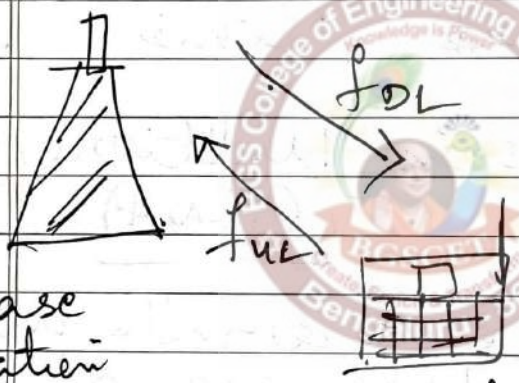
Duplexing :-

Duplexing is a technique where users send information simultaneously to base station while receiving information from base station.

Wireless telephony applies duplexing technique

→ Freq Division Duplexing :- (FDD)



Signal from mobile to BS is uplink and BS to mob is downlink.

In FDD BS will transmit & receive at same time but using diff freq's.

→ Time Division Duplexing (TDD)

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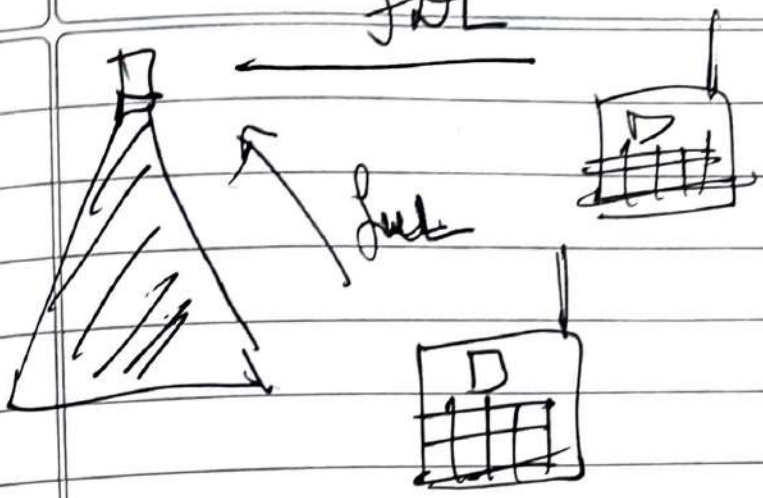

BS transmit & receive signals on the same freq but at different times.